論文の内容の要旨

論文題目 Low-power Nano-meter CMOS Circuit Designs with Application to FPGA
（低電力ナノメートル CMOS **回路設計とその** FPGA **への応用）**

氏名 **チャン　クワン　カイン**

Integrated circuits (ICs) have advanced remarkably during the past 35 years and today an IC usually have more than one million transistors, called large scale integrated circuit (LSI). LSI can be found in computers, cellular phones and other digital appliances that exit everywhere. LSI has become absolutely necessary in people life, become indispensable element to realize the ubiquitous society. LSI is expected to continue progress more and more, but coming to these days it faces some problems such as power consumption, development time and cost, process variation, etc. In the state-of-the-art technology, power dissipation of one high-end processor exceeds 100 W, and leakage power accounts for more than 50% of total power. Many methods such as clock-gating, dual-V_{DD}, dual-V_{TH}, MTCMOS (Multi-threshold CMOS), VTCMOS (Variable Threshold CMOS), Super Cut-off CMOS, Super Cut-off Zigzag CMOS, V_{DD} hopping, etc. have been proposed to reduce power consumption, especially leakage power. Thanks to these techniques, power consumption of LSI has been reduced to a degree that can be accepted for now. However, to make the progress of LSI continue in the next ten years, to secure the device reliability and to extend the battery life of mobile devices, more two orders of magnitude reduction of power consumption is assumed to be necessary. Another problem is the development time and cost. The development time

and cost have increased explosively and today they could be more than one year and one million dollars, respectively. In order to solve the development time and cost issue, some programmable LSIs such as FPGA, reconfigurable processor, etc. have been proposed. The programmable LSIs usually have more transistors than other LSIs in order to achieve the programmability. Therefore, they consume more power than the others. In this thesis, low-power especially low-leakage circuit design methods with the application to FPGA are investigated.

First, low-power high-speed level shifters are proposed. In the proposed level shifters, because the contention between the pull-up transistors and pull-down transistors is mitigated, the crow-bar current becomes smaller. Therefore, power and delay are smaller than that of the conventional level shifter. The measurement results when 0.35μm CMOS technology is used, shows that power and delay can be reduced by 50% and 65%, respectively.

Second, the basic logic element of an FPGA, CLB (Configurable Logic Block), with low-leakage current is proposed. In the proposed CLB, sneak leakage issue is dealt. Simulation using 0.15μm CMOS technology shows that leakage current of the proposed is reduced by two orders compared to that of the conventional CLB.

Next, low-leakage low-power FPGA architecture is proposed. In the proposed FPGA, low-swing interconnect and the proposed level shifter, CLB are adopted. Four CLBs are clustered into one block. A test chip fabricated in 90nm CMOS technology shows that dynamic power of the proposed FPGA can be reduced by 82% compared to that of the conventional FPGA when the speed is half of the achievable maximum speed. Leakage power of the proposed FPGA can be reduced by 89%.

Finally, a CAD for low-power FPGA is proposed. VPR is the commonly used CAD for studying FPGA architecture but it does not have a model to estimate power consumption of FPGA. A power model has been proposed by a group from the University of British Columbia called UBC Power Model. This model is included in the VPR and can be used to investigate many kinds of FPGA which have the island style architecture. However, the UBC Power Model is for only FPGAs with a single supply voltage. A new CAD that available for the use of dual-V_{DD}, low-swing interconnect, Zigzag power-gating and level shifter is proposed. Simulation using the proposed CAD with MCNC benchmark circuits shows that, power consumption of the proposed FPGA which includes dual-V_{DD}, low-swing interconnect, Zigzag power-gating and level shifter can be reduced by 57.4% on average.