論文の内容の要旨

Modeling and Characterization of Electrical Behaviors of Interconnects in Deep Sub-micron VLSI's
（ディープサブミクロン VLSI における配線の電気信号特性とそのモデリングに関する研究）

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Abstract:

Signal integrity has become a more serious issue as VLSI's scaling of technology continues into deep sub-micron region. While scaling of transistors results in faster yet low-power circuits, shrinking the physical size of interconnect may restrict VLSI's performance. Previously neglected interconnect inductance seems to have become the cause of various signal integrity issues such as propagation delay error, overshoots, and crosstalk due to coupling effects. In this dissertation, the behaviors of inductive interconnects are investigated.

First, modeling of single and parallel VLSI's interconnects are employed. Output response of single inductive interconnect is modeled. An approximation function of the model is proposed in quadratic delayed transfer function. Using proposed approximation function, which is able to be transformed to closed-form time domain function analytically, the voltage waveform of inductive interconnects can be calculated simply. It is also shown that by transformation of variable, proposed approximation function can be expressed using only one parameter, *A*. Interconnects are less inductive or behave as *RC* interconnects when *A* is less than 1. Otherwise, inductive effect may need to be considered. Moreover, formulas of the peak of overshoot time and voltage, as well as attenuation constant and peak-to-peak time are also derived in very simple forms. Also, a closed-form propagation delay formula is proposed. Additional study about distributed model of interconnect is also given.

Furthermore, the study is extended to modeling of parallel interconnects. The case of two adjacent interconnects, which consist of aggressor and victim lines, with inductive and capacitive coupling is studied. Output responses of two-adjacent coupled interconnects are modeled into two transfer functions, so-called fast and slow waves. Aforementioned proposed approximation function is applied for fast and slow waves. Finally, closed-form functions of output responses of both aggressor and victim lines are calculated with the summation and difference between the fast and slow waves.

The second part of this dissertation is discussing the effects of inductive effects in deep sub-micron region as well as in the previous technologies. The trends of inductive effects in deep sub-micron VLSI's are studied for the optimal buffered interconnect by investigating the propagation delay deviation, output response, and power consumption distribution. In optimal buffered interconnect, big driver and long enough line are used to make interconnect more inductive. The study shows that global layers interconnects, which lay on the upper layers,

suffer from inductive effects much more than local layers interconnects, which are close to the cells of transistors. Also, it is known that inductive effect increases as interconnect width increases. For optimally buffered interconnects, error due to inductive effects is less than 10% in 90nm-technology, when interconnect width is less than five times of minimum interconnect width, and the error decreases as scaling of technology continues. Furthermore, the trend of maximal value of inductive index for past, present, and future technologies are calculated from the past 1.2μm-technology to the future 22nm-technology. The result shows that previously inductive effect was neglectable but had been increasing until before entering deep sub-micron region. Later, the inductive effect is gradually decreasing in more advanced technologies. This trend explains why previously VLSI's designers did not consider inductive effects, while from this study on inductive effects in optimally buffered interconnects, the effects are gradually decreasing in deep sub-micron VLSI's.

Finally, to verify the signal integrity issues in the VLSI's, measuring the characteristics of on-chip interconnects is required. However, measuring the waveform on the lower-level interconnects from the outside of the chip encounters many difficulties due to the higher-level metals that block the access to the lower-level metals physically and electrically. Thus, an on-chip sampling oscilloscope with very high time resolution is proposed for measuring the waveforms of interconnects. Proposed on-chip sampling oscilloscope is designed and fabricated in 90nm-technology. Measurement of interconnects waveform is then demonstrated with smoothly adjustable 1ps-to-64ps time resolution, which is enabled by sampling timing generator based on ramp waveform division scheme.