Abstract of Dissertation

Low-power Circuits and Architectures for Ultra-Wide-Band (UWB) Transceiver toward Ubiquitous Electronics Applications
（ユビキタス・エレクトロニクスに向けた UWB トランシーバーのための低電力回路とアーキテクチャ）

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This thesis proposes low-power circuits and architectures for ultra-wide-band (UWB) communication system towards ubiquitous electronics applications. The thesis is organized into seven chapters. The first chapter is motivation and goal of the thesis.

Chapter 2 introduces definitions of UWB signal, regulations for UWB transmission, pulse modulation methods, and two conventional UWB systems. The first architecture is a correlator-based UWB system which precise synchronization is required. The second one is match-filter-based UWB architecture. This system does not need the precise synchronization but it requires an ultra-high-speed analog-to-digital converter (ADC) to digitize the incoming pulse for performing pulse-position demodulation by a match filter.

Chapter 3 proposes a new architecture of pulse-based UWB communication system. The architecture is named as 'Double Thresholding' method which is suitable for binary phase shift keying (BPSK) modulation scheme. The proposed architecture requires only front-end amplifiers, continuous-time comparators, digital bit holder and a phase detector (PD). Any incoming pulse is amplified before comparing with two threshold levels at the comparators to detect positive and negative peaks. The PD decides bit of the received pulse from the first rising edges when the peaks are detected. Since only first rising edge is considered, the architecture can ignore any multi-path signal as well. Bit-error-rate (BER) performance of the system is also better than previous methods because the two threshold levels generate a noise gap which makes the system can tolerate very high noise floor.

Many circuit innovations for implementing the double thresholding UWB transceiver are explained in chapter 4. A parallel common-gate amplifier with resistive termination is used as the front-end amplifier, and then three parallel common-source stages are used to enhance total gain of the amplifier. The resistive termination of the most front-end block enables wideband impedance matching with low power consumption, but it has poor noise figure of 20.3dB. Fortunately, the proposed double

thresholding architecture has very good noise resiliency and this level of noise figure is acceptable in the proposed architecture.

A low-power opamp with source-degenerated active-load compensation is also proposed in the chapter 4. This opamp eliminates feed-forward path while the feedback loop still exists. This opamp is used in a direct current (DC) voltage stabilizing loop of parallel current-reused amplifiers which DC voltage at the output node is not stable. Thus, the opamp does not require high slew rate, but it must has very small bandwidth and low power.

A short-active long-sleep style clocking architecture, which is called as 'Flashing', is applied into analog parts of the UWB transceiver in this thesis to utilize power of the pulse-based UWB system since the pulse width is very narrow compare with period of two adjacent pulses. Two fast wake-up approaches are proposed here. The first one is to use small replica circuits to keep DC operating point at the output node of flashing circuits. The small replica bias circuits are called as 'Bias keeper' and they consume much less power than the core analog circuits. When the core analog circuits are down into sleep mode, the bias saver is still active. It suddenly recovers operating voltage after the core circuits turns to active mode. The second method is to apply some delay for clock of each amplifier stage. The earlier stage is firstly turned on and the later stages are turned on after delay. For four stage amplifiers, this staggered activation scheme can reduce total wake-up time down to 56% of the non-staggered scheme.

Chapter 5 shows an implementation of the proposed circuits and architectures in a micro-power flashing UWB transceiver. The proposed UWB transceiver is manufactured in a 0.15 m FD-SOI CMOS technology and the measurement results are shown in this chapter. The proposed UWB transceiver achieves power consumption of 299 W with speed of 25kbps at distance of 35cm under 1-V supply voltage. This speed is five times higher than other micro-power transceiver.

Chapter 6 gives many discussions on performance improvement of the UWB transceiver for ubiquitous electronics applications. A new structure of LNA is proposed in this chapter. This LNA structure has a common-gate input structure to achieve wideband impedance matching, while gain of the LNA can be achieve from a feed-forward gain which is parallel common-source structure. Since impedance matching and gain can be separately designed, the LNA is named as 'matching-separated LNA'. This LNA structure is very easy to design due to separation of the matching and gain. At the same distance, improvement on BER is estimated around 1000 times better than using the amplifier with resistive termination. For other alternative of improvement, the three

times longer distance with the same BER level can be expected by using the matching-separated LNA.

A compact outside-rail circuit structure is proposed for using in an outside-rail UWB pulse transmitter. The compact outside-rail structure has only two transistors per one nominal supply voltage (VDD) while the conventional structure requires six transistors. An outside-rail opamp and an outside-rail filter are demonstrated as examples of analog part in ubiquitous electronics applications. For supply voltage of nVDD, the transmission distance can be expected to be n times longer by using the outside-rail pulse transmitter. For analog part of the ubiquitous applications, the estimated die area can be scaled down to n-2 factor.

Finally, conclusions are made in the last chapter of the thesis.