Abstract of Dissertation

Study on Noise Immunity of Low-Power Static CMOS Digital Design

（低電力スタティック CMOS デジタル設計における ノイズ耐性に関する研究）

モハメド　アパス　アボドロラヂ　アボドロハメド

Abstract:

In the past, noise was not such a big issue in digital integrated circuits. However, the continuous progress in semiconductor technology put the noise issue among the major concerns of digital CMOS IC designers. This study concerns with the noise immunity of static CMOS low power digital design by investigating the noise immunity of the current low power static CMOS design schemes and presenting a fast and accurate methodology to evaluate the noise sensitivity of the different nodes in a design during the design phase. In addition, for the modeling/characterization of noise in digital circuits, techniques to measure the non-periodic noise and sensing the peak minimum/maximum fluctuation on-chip have been presented. The study is presented in five chapters in addition to conclusion.

The first chapter includes a background about the power consumption and noise issues in current and future VLSI/ULSI digital design. It also includes the objectives of the study and thesis organization.

In chapter two, we present the effect of noise on the performance of a selected group of low power as well as traditional digital design techniques. First, we present a model for the different noise sources in the digital circuits. Then we applied the model to a selected group of low power and traditional designs as testing circuits. The noise immunity of the tested schemes has been reported in terms of logic error and delay error. At the end of the chapter, we present a methodology for leakage power saving and at the same time has high noise immunity. One of the ways to increase the noise immunity of a digital circuit is to give special strengthen considerations to the soft (weak) parts (nodes) against noise. Since it is time consuming to analyze the noise-sensitivity of different nodes in a big design using transistor level simulators, an analytical (fast and accurate) method is required.

In chapter three, we present a methodology to evaluate the noise-induced logic error probability in a given CMOS digital design in terms of supply voltage, threshold voltage, noise level and circuit configuration. At first, we modeled the noise immunity of the different logic

gates in terms logic error probability including the effect of supply and threshold voltage, which is called electrical masking. Then, time masking has been modeled to include the variation of the spurious pulse width and generation time in the overall logic error probability. Moreover, the logic masking effect has been also considered. The electrical, timing and logic masking have been combined to form the overall logic error probability model. The model has been used to evaluate the logic error probability caused by the noise at the different nodes in digital circuit examples. The model results have been compared with results obtained from HSPICE simulation. The results reveal that the model fit with the expected simulation results achieving speedup factor of more than 1000 over HSPICE. Moreover, the calculation time of the methodology is linearly proportional with the number of gates in a design, and hence, the method is suitable for investigating the noise immunity of the big circuits. The model can be used to identify the weak parts against the noise in a given design during the design phase and hence it helps the designer in giving specific design considerations to strengthen the weak nodes. The methodology is based on hypothetical noise distribution. So that, for more accurate results, a real noise distribution should be provided.

In chapter four we present, first, an overview on the previous works regarding the on-chip noise measurement has been given. To avoid the problems attached with the previous designs, an on-chip noise detector has been designed and fabricated using 0.18μm technology. The detector can detect the single-event or the non-periodic signals within the measurement time window. It is equipped with a programmable voltage divider to be able to detect high-swing signals having maximum theoretical frequency of 5GHz. The bandwidth of the output signal can be controlled by the user to fit the monitoring tools capability off-chip and to avoid the effects of the on-chip parasitic elements and hence conventional equipments can be used to measure the signal off-chip. Moreover, the detector is synthesizable and the designer can flexibly adjust its main parameters. A test chip is fabricated and tested successfully. The detector's design has been modified to increase the sampling rate. Upon the simulation results, the modified version is capable to measure signals of frequency (theoretically) up to 10GHz.

Chapter five includes the description of a CPU-interfaced system to monitor the minimum/maximum fluctuation in both VDD and ground in a design. In addition to the magnitude information, the system has the ability to report the timing and spatial information of the spurious pulse. The system is designed using Rohm 0.18μm technology. The fluctuation is detected by comparing with a reference voltage supplied form off-chip, and the fluctuation information is send off-chip in digital format. The detector is simple, therefore, it can be replicated within a design to detect the fluctuations on VDD/Ground net at different spots and

hence, safe operation can be guaranteed. The detector is interfaced by a CPU and hence it is suitable for future VLSI/ULSI circuits.

Finally, we conclude the study in chapter six.