Abstract of Dissertation

Study on Front-End ASIC for PET Detector
PET 検出器用フロントエンド回路の研究

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1. Introduction

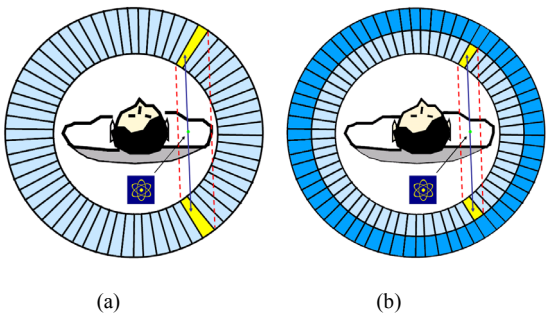
In PET, a high sensitivity (percentage of radiation detected) to reduce exposure to patients and a high spatial resolution for clearer images is desired. However, the spatial resolution of commercial clinical PET scanners is about 4~6 mm which are inferior compared to other medical imaging modalities such as CT (Computed Tomography) and MRI (Magnetic Resonance Imaging) with sub-millimeter resolution. In the case of small PET systems dedicated for use in animal studies with small animal like rodents, the spatial resolution have improved considerably over these few years but the improvement in sensitivity has not been able to follow suit.

Both the sensitivity and spatial resolution can be improved by using small scintillating crystals and photodetectors with individual readouts but this would greatly increase the number of readout channels which is impractical with conventional front-end electronics made up of discrete components. Thus, in an attempt to improve the two factors, several highly integrated Application Specific Integrated Circuit (ASIC) front-end electronics have been developed using 0.35 μ CMOS technology for individual readouts of finely granulated detector module.

2. Next Generation PET detector module

2.1 Detector module with DOI decoding

DOI decoding improves spatial resolution in areas away form the center of the camera as explained in Fig. 1. The new detector module that has been proposed is shown in Fig. 2. Scintillating crystals of different decay time are stacked and readout with a multi element APD to allow depth-of-interaction (DOI) decoding through pulse shape discrimination. Since this scheme greatly increases the number of channels, ASIC, being highly integrated, reliable and power efficient, will be used as an alternative to bulky discrete conventional electronics.



(a)　　(b)

Fig. 1. Inability to tell along which depth of the crystal the gamma ray interacted causes degradation of spatial resolution. Parallax error with no DOI information (a) and with DOI information (b).

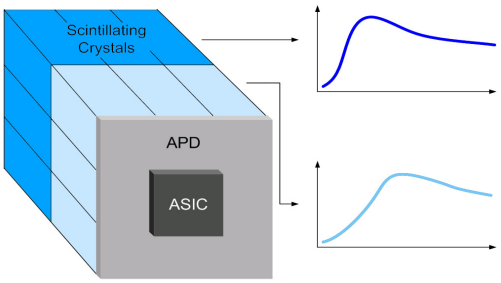


Fig. 2. Proposed detector module. Difference in decay time of crystals enables DOI decoding.

2.2 ASIC front-end electronics

Application Specific Integrated Circuit (ASIC) is a family of IC technology that is designed for a specific purpose. They are indispensable especially in applications where readout s　of large number of channels are needed and the use

of discrete electronics would be prohibitive due to cost, space and power consumption constraints. Using ROHM 0.35 μ CMOS technology through VLSI education and development center (VDEC) of the University of Tokyo, several ASIC front-end electronics has been designed for readout of radiation detectors.

3. ASIC design and experiments

3.1 Multi-channel preamplifier chip

A preamplifier is the most fundamental component in front-end electronics of radiation detectors. A 10-Ch and a 16-Ch Application Specific Integrated Circuit (ASIC) preamplifier chip with telescopic-cascode topology and gain-boosted (regulated) cascode topology respectively has been designed for readout of Avalanche photodiode (APD). These chips were fabricated on a 2.4 mm x 2.4 mm die area and micrograph of the 16-Ch chip is shown in Fig. 3. The summary of the test results of both chips is presented in Table 1.

Table 1. Characteristics of the preamplifier chips

Parameter	10-Ch chip	16-Ch chip
Gain	0.7/pF	0.9/pF
ENC (0.5 μs)	900 e^- + 60 e^-/pF FWHM	900 e^- + 75 e^-/pF FWHM
Linearity	< 2.5% (-0.5 pC to 1.2 pC)	< 0.5 % (-0.5 to 1.5 pC)
Rise time (10% - 90%)	15 ns	13 ns
Power consumption	200 mW	70 mW

Both chips have also been used to readout an APD (Hammatsu S8644-55) coupled to a GSO scintillating crystal. An optimum energy resolution of 11.3 % FWHM for the Na-22 annihilation peak was attained at an APD bias of 370 V (gain ~ 60) and 0.5 μs shaping time (Fig. 4). The experimental setup for time resolution of two coincident GSO-APD detectors is shown in Fig. 5 and the time resolution was measured to be 12.5 ns. 3 bare preamplifier chips have been fabricated into a 48-Ch preamplifier board to be used in various experiments. Although primarily designed for APD, these chips can also be used with other detectors if conditions are similar. The 16-Ch chip has been successfully used to readout a 3 cm x 3 cm Microstrip Gas Chamber (MSGC) and a 20.5% FWHM energy resolution of a Fe-55 source (5.9 keV peak) was obtained.

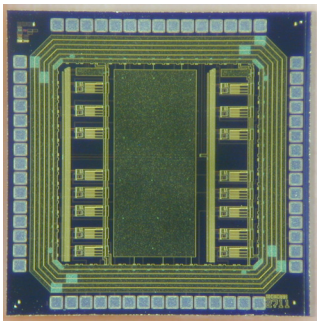


Fig. 3. Micrograph of the 16-Ch preamplifier ASIC chip.

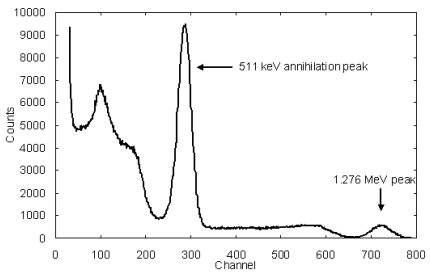


Fig. 4. Energy spectrum of Na-22.

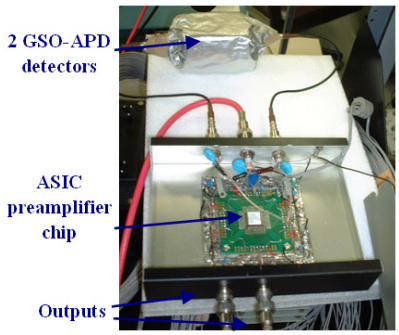


Fig. 5. Experiment setup for time resolution.

3.2 Novel Waveform Sampling Front-End (WSFE) chip

Based on two prototype WSFE chips, a new 9-Ch (including 1 test Channel) chip has been designed. Each channel of the chip consists of a preamplifier, a variable gain amplifier (VGA) and a fast analog to digital converter (ADC) with digital encoders. The preamplifier picks up detector signals and feeds them to the VGA, which adjusts the amplitude to the maximum input range of the ADC. The ADC samples the amplified signals and converts them into digital waveforms (Fig. 6). From the rise time of these waveforms that depend on the scintillating crystal decay time, DOI

information can be obtained. Such a chip, which greatly simplifies the front-end electronics and signal processing, will be the heart of the proposed detector module.

The preamplifier is based on the telescopic-cascode topology and its characteristics are summarized in Table 2. The gain of the VGA can be varied from about 5 to 16.5 via external pins. Since the ADCs consume most power in the chip, a 6-bit folding ADC has been adopted. The Folding ADC is a modification of the flash ADC that requires a smaller number of comparators. This ADC works up to 60 Msamples/s which was less than the 100 Msamples/s as designed but nevertheless should be sufficient for use in the system. The DNL and INL are 0.7 LSB and 1.4 LSB respectively.

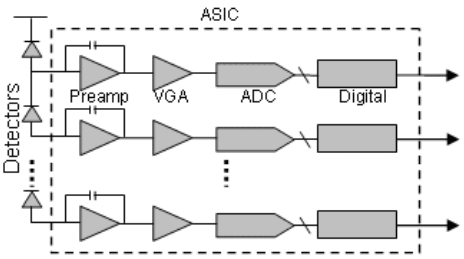


Fig. 6 Block diagram of the WSFE ASIC chip.

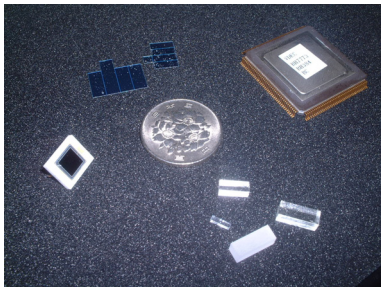


Fig. 7. Components of the detector module. Clockwise from top right: WSFE chip, GSO crystals, APD and reflectors.

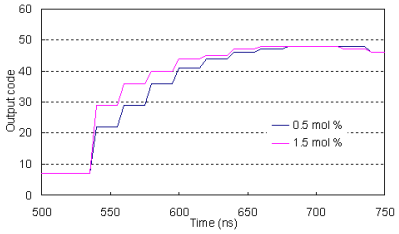


Fig. 8. Typical digitized GSO/APD at 50 MHz clock.

Since the test performance was satisfactory, one complete channel was used to assess the DOI capabilities of this chip with APD and two types of 2.9 mm x 2.9 mm x 7.5 mm GSO:Ce (0.5 mol% and 1.5 mol%) crystals of 60 ns and 35 ns decay times respectively. The key components that make up the detector module are shown in Fig. 7. 50 digitized signals samples were taken and the average rise time of each crystal was found to be 105 ns and 90 ns respectively. Fig. 8 shows that the signal from each of crystals could be differentiated from one another, thus enabling a 2 layer phoswich detector. In this experiment, the ADC was provided with a 50 MHz clock and the power consumption of the chip at this clock rate was about 1.8 W. A dedicated board with an onboard FPGA to effectively extract DOI, timing and energy information has also been developed (Fig. 9).

Table 2. Preamp characteristics in WSFE chip

Parameter	Characteristics
Gain	1.2/pF
ENC (0.25 μs)	1150 e^- + 35 e^-/pF fwhm
Linearity	< 0.5 % (-0.6 to 1.5 pC)
Rise time	19 ns

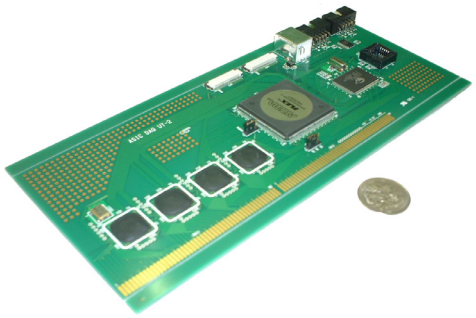


Fig. 9. Dedicated data aquisition board (40 channels) made with 4 bare WSFE ASIC chips and an embedded FPGA.

3.3 12-Ch Preamplifier-Shaper-Discriminator chip

A 12-Ch (including 2 test Channels) Preamplifier-Shaper-Discriminator ASIC has been designed and fabricated on a 2.4 mm x 2.4 mm die area. The block diagram of this chip is shown in Fig.10 and the micrograph is shown in Fig. 11. Both analog and digital components are present and a window type discriminator was implemented through the use of a digital encoder to encode outputs from two comparators. This versatile chip can be in a low cost PET system without DOI information or simply as counters.

The charge sensitive preamplifier of this chip is based on gain-boosted (regulated) cascode topology as implemented

in one of the preamplifier ASIC chip described above. The gain of the preamp-shaper is 2.5/pF and the shaping time can be varied from about 0.3 μs to about 0.8 μs via an external bias. The linearity of this chip is less than 1% up to 320 fC for negative charge and 150 fC for positive charge. Fig. 12 shows typical shaper output signals obtained with different input charges. The noise of a complete chain (preamplifier-shaper-discriminator) has been determined to be about 1500 e^- + 75 e^-/pF rms and the power consumption of the chip is 0.13 W.

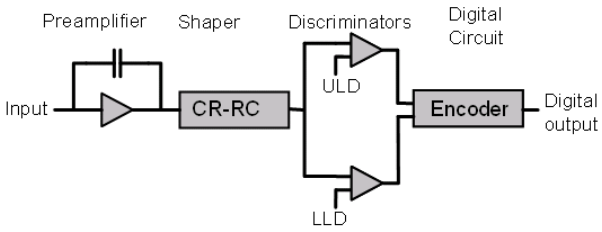


Fig. 10. Block diagram of a single Channel of the 12-Ch Preamplifier-Shaper-Discriminator ASIC chip.

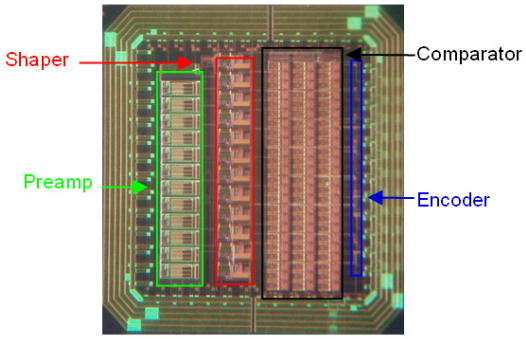


Fig. 11. Micrograph of the Preamplifier-Shaper-Discriminator chip

The Time over Threshold (ToT) has also been measured for all working channels (except test channels 0, 1 and 10, 11 which were not working) for various input charges as shown in Fig. 13. Some systematic variation of ToT which is inevitable due to the technology process was observed. Thus, individual threshold (ULD and LLD) input for each channel rather than a common threshold for the whole chip would improve its applicability.

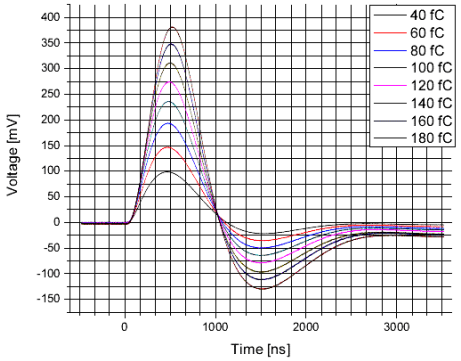


Fig. 12. Shaper outputs for various input charges.

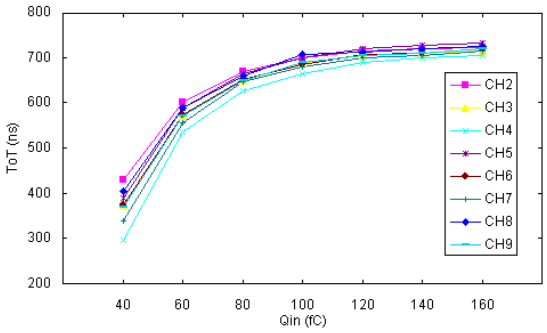


Fig. 13. Time over Threshold (ToT) versus input charge.

3. Conclusion and further studies

A new PET detector module designed at maximizing sensitivity and achieving spatial resolutions near theoretical limits, has been proposed and several ASIC chips for use with radiation detectors have been fabricated. The multi-channel preamplifier chips, especially the 16-Ch preamplifier, work well and have been put to practical use. A new WSFE chip has been fabricated and has shown to be able to differentiate signals from at least two types of GSO signals for different decay times. A more quantitative method of comparing the rise times through the use of FPGA and complex statistic estimators might lead to better distinction of these slopes and allow a 3 layer phoswich detector. Performance in all areas (spatial resolution, count rate and energy resolution) can be expected to improve if this chip is implemented into a PET system. As for the 12-Ch Preamplifier-Shaper-Discriminator, each component was working although some modifications may be needed. The baseline return of the shaper was quite slow at around 4 μs (Fig. 12) which might cause pile up at high counting rate and some systematic deviations in the ToT amongst channels, inevitable due to the technology process, was observed.