Abstract of Dissertation

Optimal Generation of Design-Specific Cell Libraries
(設計固有セルライブラリの最適生成手法)

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This dissertation focuses on optimal generation of design-specific cell libraries. In cell-based integrated circuit design, a cell library defines the final quality of a design. Hence, use of a general-purpose cell library may lead to a poor quality. We address various issues regarding optimal generation of design-specific cell libraries, targeting high-performance digital circuit design.

The goal of the first part of the dissertation is to provide the key components required to successfully realize the automatic generation of design-specific cell libraries, which consists of cell logic type selection and drive strength type selection.

Chapter 2 addresses feasibility issues on transistor-level optimization. During transistor-level optimization, cell layout synthesis and characterization steps are the major bottlenecks with respect to runtime. To resolve this drawback, we present a fast and accurate prelayout estimation technique of cell characteristics. Our estimation technique is based on quick transistor placement. Given a transistor-level circuit of a cell, layout parasitics are estimated using quick transistor placement. Then, the cell is characterized by simulating an estimated circuit which is built according to the estimated layout parasitics. Experimental results on a 0.13um industrial standard cell library demonstrate that the proposed technique estimates the cell characteristics with a reasonable accuracy in a negligibly small amount of time.

Chapter 3 addresses a cell logic type selection problem for design-specific cell libraries. Our methodology consists of two steps: logic-rich cell library generation and cell logic type count minimization. We propose a cell logic type count minimization method which minimizes the logic type count iteratively under performance constraints. Experimental results on the ISCAS 85 benchmark suite in an industrial 90nm technology demonstrate that it is feasible to find the minimal set of cell logic types under performance constraints.

Chapter 4 addresses a performance-constrained cell count minimization problem for

continuously-sized circuits. After providing a formal formulation of the problem, we propose an effective heuristic for the problem. The proposed hill-climbing heuristic iteratively minimizes the number of cells under performance constraints such as area, delay and power. Experimental results on the ISCAS 85 benchmark suite in an industrial 90nm technology demonstrate its effectiveness. We also discuss several implementation issues towards a practical application of the proposed method to large-scale circuits.

The second part of the dissertation focuses on transistor-level topology synthesis, which is an important component in the manual generation phase where portions of a circuit are manually identified and cells for the portions are synthesized at the transistor level. We present three transistor-level topology synthesis methods. Although their objectives are to minimize the transistor count, they have different solution spaces. Combining these methods, the minimum solution in larger solution space can be obtained.

Chapter 5 presents a method for synthesis of minimal static CMOS circuits where the solution space is restricted to the circuit structures which can be obtained by performing algebraic transformations on an arbitrary prime-and-irredundant two-level circuit. The circuit structures are implicitly enumerated via structural transformations on a single graph structure, then a dynamic-programming based algorithm efficiently finds the minimum solution among them. Experimental results on a benchmark suite targeting standard cell implementations demonstrate the feasibility of the proposed procedure. We also demonstrate the efficiency of the proposed algorithm by a numerical analysis on randomly-generated problems. It is also shown that the proposed procedure sometimes generates significantly smaller circuits compared to conventional approach.

Chapter 6 presents an exact method for minimum logic factoring which can be viewed as the synthesis of a static CMOS compound gate. We first introduce a novel graph structure, called an X-B (eXchanger Binary) tree, which implicitly enumerates binary trees. Using this X-B tree, the factoring problem is compactly transformed into a quantified Boolean formula (QBF) and is solved by general-purpose QBF solver. Experimental results on artificially-created benchmark functions show that the proposed method successfully finds the exact minimum solutions to the problems with up to 12 literals.

Chapter 7 studies the synthesis of read-once switch networks in which every variable appears only once. The proposed procedure is based on the notions of prime implicants and unateness, which establish a basis for Boolean expression synthesis. We also propose a

pruning technique for an efficient search. Experimental results on randomly-generated problems with up to 20 switches demonstrate that the proposed procedure successfully solves about 90% of the problems in 10 minutes each and the resulting read-once switch networks are up to 78% smaller compared to series-parallel switch networks.

Chapter 8 conducts an experimental study using a circuit consisting of C432 and C499 from the ISCAS 85 benchmark suite as a design example. We compare the circuits synthesized with a typical cell library and optimal design-specific libraries in an industrial 90nm technology, and demonstrate that using the design-specific cell libraries, the area-delay tradeoff curve is shifted to the left-bottom from that using the typical library. Comparing between the area-optimal circuits, the area is improved by 27.3%. And, comparing between the delay-optimal circuits, the maximum delay is improved by 22.4%. These results clearly prove the effectiveness of the flow and the key components for optimal generation of design-specific cell libraries.