論文の内容の要旨

論文題目　“**Image Processing VLSI Circuits for Real-Time Recognition Systems**”

(実時間認識システムのための画像処理 VLSI 回路技術)

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(本文)

Real-time object recognition is becoming increasingly important in various applications such as security systems as well as in establishing more robust and flexible human-computer interfaces. In image recognition, a target image is firstly converted to a reduced format called a feature vector, then being recognized using some sorts of classifiers. Feature extraction from an image involves a series of filtering operations, which, in general, are repeated pixel by pixel to scan the entire image. Therefore, it is computationally very expensive. In order to achieve a real-time performance in image recognition, software processing running on general-purpose processors is not sufficient in terms of speed and power dissipation. Therefore, for the purpose of real-time image recognition with high power efficiency, developing dedicated processors is quite essential.

Being inspired by the biological principle, a directional edge-based feature vector representation algorithm was proposed and has been successfully applied to medical radiograph analysis as well as to handwritten pattern recognition. Other representations also developed based on the directional edge information have been proven very robust in face detection and face identification. However, the directional edge detection costs a lot for computation. This is because the processing needs be repeated pixel by pixel to cover the entire area of the "recognition window", the sectioned image defined for partial image recognition. Furthermore, in the object search in a scene the recognition window itself must scan a large search area also pixel by pixel in the scene, making real-time processing unrealistic.

In order to realize the high-speed image recognition, seamless feature vector generation coherent to the continuous scanning movement of the recognition window is quite essential in carrying out objects search and recognition in a large scenery image. In this work, an arrayed-shift-register architecture has been employed in conjunction with a pipelined directional-edge-filtering circuitry. Four-directional edge information is detected from a 5x5-pixel block input image in coherent with the threshold determination for edge filtering. The detected edge flags are temporarily stored in a 64x64 two-dimensional array of shift registers directly linked to summation units to construct feature vectors. With this architecture, it has become possible to scan an image, pixel by pixel, with a 64x64-pixel recognition window and generate a 64-dimensional feature vector in every 64 clock cycles.

In the edge-based image vector generation, determining the threshold value for edge detection adaptive to local luminance variances is of paramount importance to perform robust image recognition. In our system, all 40 absolute-value differences between two neighboring pixels are calculated in both vertical and horizontal directions in a 5x5 filtering kernel and the median value is employed as the threshold.

Median filter is known as a very powerful rank-order filter but computationally very expensive, making the threshold determination the bottleneck of our system. This is because it requires in principle the sorting of a large number of numerical data. In order to expedite the processing, small-latency VLSI median filters have been developed using both digital and analog circuit technologies. In the digital approach the circuit is configured as a sorting network composed of a number of comparators, thus consuming a lot of chip area. In addition, power dissipation due to the long interconnects with repeaters and buffer circuitries also presents a problem. In the mixed-signal approach, on the other hand, the median filter is implemented based on binary search algorithm. The circuit is composed of majority voting circuits and simple logic circuits. In order to establish high-speed and low-power median search, high-performance majority voting circuits have been developed employing the floating-gate MOS technology.

My dissertation research has resulted in feature-extraction and vector-generation VLSI circuits for real-time image recognition. By employing arrayed-shift-register architecture, seamless scanning of the recognition window has been achieved. In order to determine the threshold for edge-filtering operation adaptive to local luminance variances, a binary median search algorithm has been implemented using high-precision majority voting circuits working in the mixed-signal principle. The prototype chip was fabricated in a 0.18-um CMOS technology. A high-speed feature vector generation in less than 9.7 ns/vector has been experimentally demonstrated using the fabricated chip. It has become possible to scan an entire VGA-size image using the 64x64-pixel recognition window at a rate of 5 frames/sec., thus generating as many as 1.5 million feature vectors in a second for recognition. This is more than 10,000 times faster than software processing running on a 3-GHz general-purpose processor.