論文内容の要旨

論文題目

DESIGN AND MODELING OF MILLIMETER-WAVE CMOS FOR WIRELESS TRANSCEIVERS
(無線トランシーバ用ミリ波 CMOS の設計とモデリングに関する研究)

氏名　ライ　チー　ホン　イワン
Lai Chee Hong Ivan

The history of millimeter-wave began from the time of Maxwell's predictions with his famous equations. History of the silicon integrated circuit developed separately from the 1960's. These two fields merged in the 1990's when the operating frequency of silicon circuits reached high gigahertz to make possible CMOS millimeter-wave circuits today. This research focuses on the use of CMOS 90nm process technology to implement millimeter-wave circuit building blocks for the wireless transceiver.

The high frequency analog portion of the wireless transceiver consists of the amplifiers, mixers and oscillators, each performing a specific function according to their roles in either the transmitter or receiver. The design of each block is not trivial, considering the frequency and power requirement objectives for CMOS implementation. In addition, the interconnections will severely affect the performance of the devices. Therefore, simply interconnecting working devices are not trivial. In order to accomplish the research work, designs are made with the help of various software, including the high frequency simulation software, Hewlett Packard's Advanced Design System (HP ADS). Chip layout for mask design is made with the Cadence's

Layout Editor software together with its verification tools. Measured results are obtained with the carefully-calibrated use of various chip measurement equipments, including a 110-GHz vector network analyzer. Each of the transceiver's building blocks have been explained with some of the most important ones fabricated and measured.

In certain parts of the transceiver that operates at lower gigahertz frequency, the on-chip spiral inductor is used. In order to use the on-chip inductor effectively, accurate and efficient models are needed. In this work, a broadband model suitable for simulation beyond the self resonant frequency is introduced with the use of fitting equations. These fitting equations are generated through an evaluation of the physical currents flowing in the substrate and at different parts of the inductor. Important fitting techniques using linear and geometric programming on nonlinear monomial equations are explained. Test structures to verify the model have been measured using a 0.35μm CMOS process and a SOI 0.15μm process.

The transmission line is another integral part of the transceiver which has to operate up to very high frequency. New low loss transmission lines up to 110 GHz have been developed. The development of these structures is based on the slow-wave propagation characteristics in the SiO_2-Si interface. However, instead of relying on material properties (substrate resistivity) to obtain slow waves, we used innovative layout designs to achieve it. The design of the slow-wave transmission line (SWTL) and an asymmetric coaxial waveguide (ACW) are described, fabricated and measured. Both structures are able to obtain a high quality factor and length reduction. Measurement results show that, SWTL achieves a higher quality factor, while the ACW is able to achieve a higher length reduction factor.

The idea of the slow-wave phenomenon is extended to the design of an on-chip broadband balun operating from 26.8 GHz to 37.3 GHz. This balun has been tested and characterized for

the use in a 20-26 GHz up-conversion mixer. The balun can also be used as a power combiner or a power splitter. Analytical expressions to describe the combiner have been derived to correct errors in existing known equations and are verified by experimental data. Consequently, a 20-26 GHz up-conversion mixer is realized for the automotive radar application that employs two such baluns operating at different frequencies. This demonstration of a fully integrated single-balanced mixer fabricated on CMOS 90nm process has a measured power consumption of 11.1mW. The results obtained are comparable to mixer circuits fabricated using high performance semiconductor processes.

The down-conversion mixer is the fundamental device in the wireless receiver. A down-conversion mixer is realized for operation in the 60 GHz license-free band. Due to oxygen attenuation at 60 GHz, wireless devices at the frequency are suitable for secure short-range applications. An important concern in realizing such circuit is the chip area consumption as chip area translates to manufacturing and material cost. This circuit employs the SWTL to reduce the chip size area. The mixer employs a cascode topology with IF output boosting and is fabricated on CMOS 90-nm process. The SWTL allows physical length reductions of 47% when compared to a microstrip line of an equivalent wavelength.

To boost the signal to a sufficient level in the transceiver chain, gain amplifiers are used. A 50 GHz variable gain amplifier has been realized using the CMOS 90nm process by employing an innovative gate resonance technique on a popular cascode circuit configuration to improve the gain. Gain at high frequency is difficult to achieve because the operating frequency for amplification should only be a fraction of f_T. This technique is implemented without additional current consumption through a series resonance by using the MOSFET gate-source capacitance with an inductive element at the gate. The inductive element is realized with a transmission line that fits well on the physical layout. The dependence of the cascode transconductance on the

gate has been analytically derived and simulated. As a result, this technique can be used to boost gain of the CMOS amplifier at high frequency.

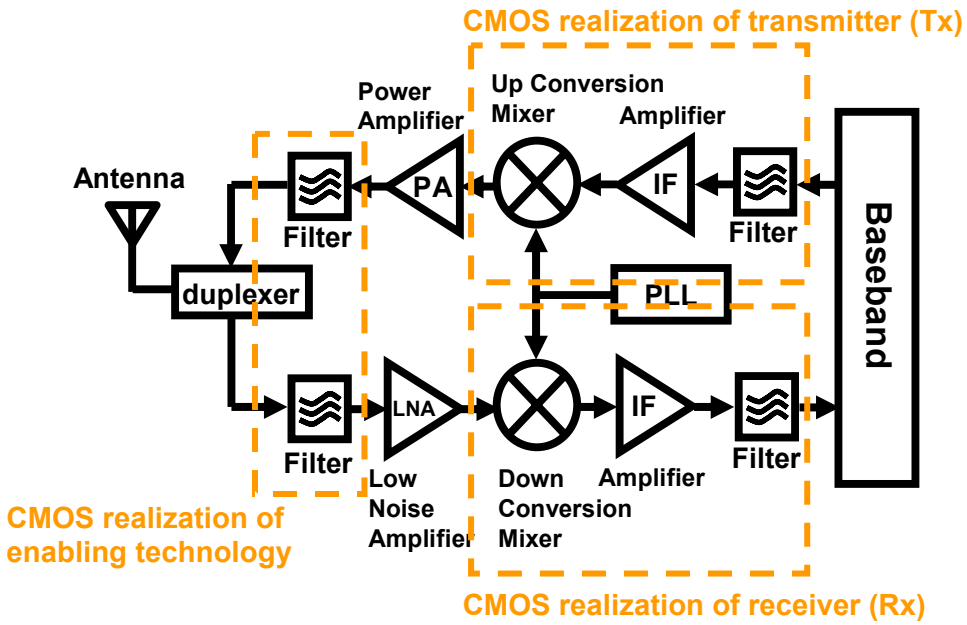

Fig. 1 The main building blocks in the RF transceiver design for the millimeter-wave band are realized.

Recall that the receiver or transmitter will almost always be realized as a string of operations where each operation is either one of these three frequency domain operations:

- *a filter*, for the suppression of signals outside the wanted channel;
- *an amplifier*, to adjust the signal level;
- *a mixer*, to change the center frequency.

In this research, the critical building blocks of the millimeter-wave wireless transceiver are accomplished. Future realization of low cost, short range (< 10m) transceivers can be fully integrated using CMOS. Mid-range transceiver (10~20m) requires high power transmission and is therefore suitable to be integrated with compound semiconductors or SiGe amplifiers. Future work is therefore expected to include the integration of the compound semiconductor

technology in addition to the continuing developments of CMOS processes and circuits.

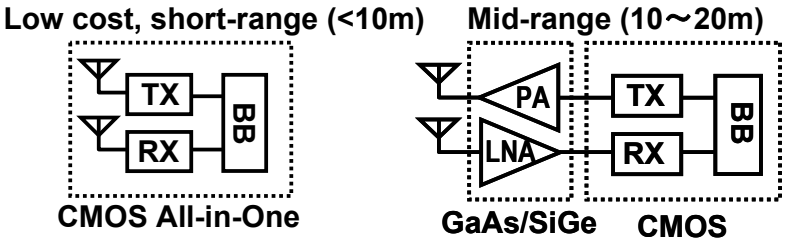

Fig. 2 Future realization of short and long range wireless communication building blocks.

The future prospect of silicon CMOS for millimeter-wave fundamentally depends on further scaling possibilities as predicted by Moore's law, the drive by consumer demands and initiatives in developing the circuits for new breakthroughs. Moore's law has consistently held true for the past 30 years and will likely continue to persist for the next decade. Process developments had overcome various obstacles and will continue to do so to sustain the infrastructure of the silicon industry. Demand for bandwidth has pushed applications to operate at a higher frequency. Hence, we can only expect the millimeter-wave frequency band uses to increase. As a start, the 60-GHz license free band is a very attractive option for consumer electronics. This will drive CMOS for millimeter-wave applications. Therefore, it is imperative to continue the development of this technology at the circuit level to meet the needs of the next decade.