論文の内容の要旨

論文題目：**Soft-Error Tolerant Cache Architectures**
(耐ソフト・エラーのキャッシュ・アーキテクチャ)

氏名：ルォン　ディン　フォン

The problem of soft errors caused by radiation events are expected to get worse with technology scaling. This thesis focuses on mitigation of soft errors to improve the reliability of memory caches. We survey existing mitigation techniques and discuss their issues. We then propose 1) a technique that can mitigate soft errors in caches with lower costs than the widely-used Error Correcting Code (ECC), 2) a technique to mitigate soft errors in Content Addressable Memories, and 3) a cost-effective cache architecture achieving both variation-induced defect and soft-error tolerance.
ECC is widely used to detect and correct soft errors in memory caches. Maintaining ECC on a per-word basis, which is preferred for caches with word-based access, is expensive. We propose Zigzag-HVP, a cost-effective technique to detect and correct soft errors for such caches. Zigzag-HVP utilizes horizontal-vertical parity (HVP). Basic HVP can detect and correct a single bit error (SBE), but not a multi-bit error (MBE). By dividing the data array into multiple HVP domains and interleaving different domains, a spatial MBE can be converted to multiple SBEs, each of which can be detected and corrected by the corresponding parity domain. Vertical parity update and error recovery in Zigzag-HVP can be performed efficiently by modifications to the cache data paths, write-buffer, and Built-In Self Test. Evaluation results indicate that the area and power overheads of Zigzag-HVP caches are lower than those of ECC-based ones.
We propose STCAM, a soft-error tolerant Content-Addressable Memory (CAM). Soft-error mitigation in a CAM is difficult due to the un-availability of data outside the cell array in a CAM access. Since CAMs are used in several components of a processor, making those CAMs being resilient against soft errors is required to attain high processor's reliability. STCAM can successfully detect and correct false hits and false misses caused by soft errors in a CAM. This is achieved through subdividing a CAM and providing backup checking for cases the input tag is partially matched in the CAM. An original encoding scheme is proposed to reduce the frequency of backup checking. Modifications to support STCAM do not increase access latency. Performance degradation incurred by backup checking is very low.
We present SEVA, a soft-error- and variation-aware cache architecture. As memory devices are scaled down, the number of variation-induced defective cells increases rapidly. Combination of ECC, particularly Single-Error Correction Double-Error Detection (SECDED), with a redundancy

technique can effectively tolerate a high number of defects. While SECDED can repair a defective cell in a hardware block, the block becomes vulnerable to soft errors. SEVA exploits SECDED to tolerate variation-induced defects while preserving high resilience against soft errors. Information about the defectiveness and data dirtiness is maintained for each SECDED block. SEVA allows only the clean data to be stored in the defective blocks. An error occurring in a defective block can be detected and the correct data can be obtained from the lower level of the memory hierarchy. SEVA improves both yield and reliability with low overheads.

Having memory caches to be tolerable from soft errors is essential for attaining high processor's reliability. Incurring low area and power overheads, Zigzag-HVP allows support for soft-error tolerance to be more affordable and therefore pervasive. STCAM increases in the coverage of soft error protection in a processor. Finally, SEVA shows that soft-error tolerance for reliability and defect tolerance for yield can be achievable with reasonable costs, paving the way for successful SRAM designs in future process technology.