論文の内容の要旨

論文題目

Circuit Technologies for On-Chip Power Supply Systems

（オンチップ電源システムに向けた電源回路技術）

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This thesis proposes lowpower, high performance and high functionality power supply circuits and architectures toward on-chip distributed power supply systems which are suitable for current and future LSI's.

The thesis is organized into 7 chapters. The first chapter includes motivation and goal of this thesis. On-chip distributed power supply system is valuable for both the power integrity issue and multiple power supply to several types of chips and circuit blocks integrated in a package. In the background, there is a fact that the optimum power supply voltage differs between different types of function blocks and they are not suppressed as technology scales down. In a distributed power supply system, power is supplied from outside the package using one high voltage and it is converted to required lower supply voltages using DC-DC converters at the vicinity of the load circuits. By doing so, the total input current for one package and power line noise issue caused by parasitic resistances and inductances are reduced.

Chapter 2 introduces three types of conventional on-chip step-down DC-DC converters. The first one is a linear regulator which is useful for on-chip implementations and suitable for applications which require low voltage ripple. Linear regulators however, have low power efficiencies when the voltage conversion ratio is low. The second one is a buck converter which performs higher power efficiency compared with the linear regulator, instead of the area overhead caused by the output LC filter and the implementation complexity. The third one is a switched capacitor DC-DC converter which is suitable for low current applications. Switched capacitor converters need an external circuit such as a linear regulator for voltage regulation. Both the operation principles and research trends on these three types of DC-DC converters are introduced in this chapter.

Chapter 3 proposes novel implementation methodologies of on-chip buck converter for higher power efficiency and lower cost. By implementing passive and active elements of a buck converter on chips or interposers in different technologies and connecting them with each other through metal bumps and vias, power and cost effective implementations are achievable. Especially two chips implementation and two chips

plus one interposer implementation are discussed in this thesis. Moreover, how to implement the switching elements which are tolerant of high input voltage is discussed. By using high tolerance voltage I/O transistors, the number of cascaded transistors can be reduced instead of over all power efficiency reduction. The optimum implementation method mixing different types of transistors for higher power efficiency and smaller area is discussed as well in this chapter.

Maintaining the supply voltage in time domain according to the required performance of the load circuit is another important aspect of power supplies especially in case of lowpower digital circuits. Chapter 4 describes the methodologies to quickly change and settle the output voltage of on-chip DC-DC converters. In case of linear regulators, voltage hopping acceleration up to ns-order of transition time is available by putting large transistors named V_{DD}-hopping accelerators in parallel with the load circuit and shorting them so quickly. By applying analog mirror delay circuit, the accelerator can be controlled robustly independent of the size of the acceleration transistors, load current and load capacitance. In case of buck converters, there occurs voltage ringing issue caused by the output LC filter when the output voltage is changed quickly by the V_{DD}-hopping accelerator. Solutions of this problem are discussed as well in the later half of this chapter. Proper timing control is one of the keys to successfully accelerate the output voltage hopping of a buck converter.

In chapter 5, a power supply circuit which performs a collaborative operation of a linear regulator and a buck converter is presented. The circuit settles the output voltage much faster than a conventional single mode buck converter, with assistance by a linear regulator put in parallel, while it achieves high steady-state power efficiencies equal to those of conventional buck converters. Proper control of the linear regulator and the buck converter achieves a smooth wake-up. The power supply works as power gating circuit for leakage current reduction of the load circuit as well.

On the other hand, inter chip wireless communication technologies using inductive or capacitive coupling are investigated aiming at lowpower and high-speed communications between stacked chips in SiP's in recent years. The communication performance basically depends on the chip-to-chip distance, and the bonding wires for power supply lines prevent them to get close with each other. By transmitting not only the signal but also the power between chips, both low assembly cost and higher communication performance are achievable. Circuit techniques and design methodology using inductive coupling for chip-to-chip wireless power transmission are presented in chapter 6.

Finally, the thesis concludes in chapter 7.