Abstract of Dissertation

論文題目　Study on Applications of Room-Temperature Operating Silicon Single-Electron Transistors
（室温動作シリコン単電子トランジスタとその応用）

氏名　宮地　幸祐

For the past 30 years, the size of a metal-oxide-semiconductor field-effect-transistor (MOSFET) in very-large-scale integrated circuits (VLSI) continued to scale down for higher integration and higher performance. As the gate length of MOSFETs has reached down to sub-50 nm, unprecedented technical issues have become prominent to proceed scaling of the MOSFETs.

Silicon single-electron transistor/single-hole transistor (SET/SHT) is one of the most promising devices for VLSI in silicon nanotechnology; the technology that seeks new function in nano structures. Although its operation principle is different from conventional MOSFETs, its fabrication process is very similar to them. Hence, it is expected that SETs/SHTs can be easily combined with CMOS VLSI and realize high functional, ultra-low power, and ultra-high density circuits. Owing to the intensive researches on SETs/SHTs, process techniques for SETs/SHTs to operate at room temperature have been establishes. In such room-temperature operating SETs/SHTs, strong quantum effect has become pronounced and started to affect the transport characteristics. However, basic analysis and enhancement of the device performance are still required for room-temperature-operating SETs/SHTs to be used in actual VLSI circuits.

In this dissertation, characteristics of the room-temperature-operating SETs/SHTs are analyzed and their advantages are fully enhanced aiming at the actual VLSI circuit applications. The feasibilities of the proposed methods are evaluated by simulations and measurements.

In the first half of the Chapter 2, characteristics of the SETs/SHTs is introduced starting from the fundamentals of the SET/SHT physics. Coulomb blockade oscillation and other important current characteristics in SET/SHT are derived from the classical physics. For the systems that quantum mechanical effects matters, quantum level spacings should be take into account. In silicon (semiconductor) SETs/SHTs, quantum effects play important roles in their transport characteristics. NDC is supposed to be the most promising quantum effects to be utilized in novel high function circuits. In the second half, some fabrication methods of the room-temperature operating SETs/SHTs are discussed. Ultra-narrow channel MOSFETs is introduced as the best method in terms of room-temperature operation. The mechanism of the formation of the tunnel barriers and quantum dots are explained. Channel potential fluctuation in undulated ultra-narrow channel by lithography, wet etching and thermal oxidation processes are the dominant origins.

In Chapter 3, a compact analytical SET/SHT model considering the discrete quantum energy levels is proposed and developed. The model is expressed in closed-form and there is no need of numerical calculation. It successfully reproduces NDC characteristics and non-periodic Coulomb oscillations due to the finite quantum level spacings. It also shows that the accuracy is comparable to the conventional full master equation method and fits well to the measured data. The model is incorporated into the HSPICE simulation, and basic NDC circuit applications are demonstrated. The proposed analytical model is promising to provide suitable environments for designing CMOS-combined room-temperature- operating highly-functional SET circuits.

In Chapter 4, the relationship between the FWHM of the NDC and voltage gain is focused for the first time and it is found by the experiments and calculations that high gain SETs/SHTs show small FWHM in NDC. Low drain-dot coupling in the high gain SETs/SHTs is considered to be the most important factor. This result indicates that characteristics of the NDC are able to design by the basic capacitance parameters of the SETs/SHTs. From the viewpoint of applications, high-gain SETs/SHTs have great advantage to NDC circuits as well as to the standard logic circuits.

In Chapter 5, FWHM of Coulomb blockade peak is modulated in a SHT at room temperature by varying substrate capacitance through changing the substrate condition from depletion to accumulation (inversion) in a thin BOX SOI substrate. The results are also quantitatively supported by the low temperature measurements in another fabricated SHT. The electrical control of the sharpness of the Coulomb blockade peak creates great opportunity for adding further functionality to the present SETs/SHTs, such as application to the novel analog pattern matching device. Also, the guide lines to increase the proposed effects for practical use are discussed.