論文の内容の要旨

論文題目　Optimization of Nanometer CMOS LSI’s through Adaptive Control of Supply and Threshold Voltage

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Power integrity and power consumption have become a more serious issue as LSI's scaling of technology continues into nanometer region. While scaling of transistors results in faster yet low-power circuits, increased power supply current causes problem of switching for saving power consumption, which restricts the power efficiency of LSI’s. Furthermore, systematic or random variations induced by its design and process result in excessive margin and higher power consumption. To cope with this problem, an adaptive noise canceller and global power optimization scheme is proposed and investigated.

The thesis is organized into 6 chapters. The first chapter describes trends and problems in nanometer CMOS LSI’s as the background. Along scaling, the operation speed increases, on the other hand, leakage power does not scale well in nanometer CMOS LSI’s, and process variation increases along scaling, which leads to large margin to obtain enough yield. To reduce cost and power consumption, adaptive control of supply and threshold voltage is essential because these post-Si tuning technologies do not only reduce the power consumption but also improve the yield, which lead to cost reduction.

Chapter 2 introduces conventional low-power techniques for system-on-chip (SoC) systems. This includes time-domain fine-grained adaptive controls and area-domain fine-grained adaptive controls. Time-domain control is to adaptively change the supply voltage or to switch the supply voltage of specific circuit block to reduce leakage when it is not in operation and preserve performance when in operation. Various sophisticated

controls are available, though they have problem of switching noise to the supply line. This problem is treated in Chapter 3. Area-domain control is used to compensate process variation using frequency monitor and back-bias generating circuit. Conventional control of this type has large area overhead due to the bias generator, and within-die process variation is becoming more random along process scaling, which makes it difficult to implement. A solution to this is shown in Chapter 4.

Chapter 3 proposes novel power supply line noise canceller using higher voltage supply for supply voltage droop in wake-up. Proposed canceller uses additional higher-than-V_{DD} power supply, namely V_{DDH}, to allow more current flow through restricted power supply network, which enables to cancel the noise without large wire or power supply network overhead. Moreover, optimum control of the switch between V_{DDH} and V_{DD}, and the amount of the noise cancelling current are discussed. With noise cancelling current as large as the load current and slow turn-off, the canceller is stable and optimum cancelling effect is achieved.

To optimize the power consumption of CMOS LSI's, not only dynamic control of the supply voltage or switching the circuit to reduce leakage, but also coping with within-die variation to reduce excessive margin which consumes excessive power is essential. Chapter 4 proposes a fine-grained global threshold voltage optimization scheme for digital circuit. Nanometer CMOS LSI's have not only random variation but also systematic variation, which derive from both design and process variations. By dividing the circuit into blocks and applying different body-bias voltages for each blocks, both systematic variations can be cancelled. This means digital circuits have some not necessary fast part and necessary fast part, and to drive the first part in fast mode consumes excessive power. The principle and detailed design consideration and

flow are also described in this chapter.

In chapter 5, a power gating switch with MEMS technology is presented. Conventional power gating switch with CMOS technology has finite leakage current, which becomes problem especially for very low power systems. With the MEMS switch, leakage current can be cut to almost zero, though the on-resistance of the fabricated chip is high. From this, the MEMS switch is for very low power systems which can accept kΩ order of on-resistance and which cannot accept on/off ratio as low as 10^5. Furthermore, the durability of the MEMS switch is discussed in this chapter, and a circuit technology to extend its life time is also presented.

Finally, the thesis concludes in chapter 6.