論文の内容の要旨

論文題目　Cause Analysis of Threshold Voltage Variability in MOSFETs by Device Simulation
（デバイスシミュレーションによる MOSFET のしきい値電圧ばらつきの要因解析）

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The fluctuating parameters which are considered to be the origins of threshold voltage (Vth) variation in metal-oxide-semiconductor field-effect-transistors (MOSFETs) are developed and introduced into three-dimensional device simulator. Using device simulation with new developed fluctuating parameters, it makes possible to evaluate the Vth variation in real devices. Each fluctuating parameter is assumed independently to see the impact on Vth variation more clearly.

In the past couple of years MOSFETs have reached decananometre (between 10 nm and 100 nm) dimensions with 40-50 nm physical gate length devices available now in the 45 nm technology node, 32 nm transistors ready for mass production in next couple years. The gate length of the most advanced MOSFETs has already fallen below 30 nm. However, various problems that obstruct more miniaturization of MOSFETs have become prominent as the device size is aggressively scaled down. The electrical characteristic variation, such as Vth variation is one of the big issues in scaling MOSFETs. To reduce the issue of Vth variation, its origin should be clarified first. This issue becomes prominent in short channel because the fluctuating parameters are not averaged out in small size MOSFETs.

The objective of this study is to analysis the origins of Vth variation of both NMOS and PMOS in current VLSI technology. Since, it is very complicated to determine the real origin of Vth variation in short channel due to the short channel effect (SCE) and drain induced barrier lowering (DIBL), this work is focused on not-so-aggressively scaled down gate length at low drain voltage. In cause analysis of the Vth variation, Takeuchi coefficient B_{VT} is utilized, which is derived from uniformly random dopant fluctuation with low drain voltage. For estimating dopant profile effect on Vth variation, a new methodology is proposed. Using a newly proposed method, dopant profile effect on Vth variation is enhanced, so that profile impact can be observed clearly.

A very rapid method of estimating the effect of gate edge fluctuation on Vth variability in MOSFETs is proposed. An empirical model is developed, in which correlation width (Wc) from gate line width roughness (LWR) is a key parameter of the model. The validity of the model is confirmed using the measured data and an autoregressive model. Wc is extracted from the gate line edge shape depicted in a scanning electron microscope (SEM) image. This method is very useful for the intuitive understanding of the gate edge fluctuation effect on Vth variability.

Two well known dopant models for the Coulomb potential, which are atomistic model and long-range model, have been compared using device parameters in the 45nm technology node and beyond. It is found that the atomistic model has unacceptable dependences of average threshold voltage on mesh spacing and substrate dopant concentration, while the long-range model has minimum dependences. Consequently, the atomistic model severely overestimates the Takeuchi coefficient B_{VT}, which is one of the most important parameters for random threshold voltage variation. It is concluded that the long-range model is more suitable for the prediction of random variation in future aggressively scaled metal-oxide-semiconductor field-effect-transistors (MOSFETs).

Vth variations induced by oxide thickness fluctuation (OTF) and local gate depletion (LGD) in MOSFETs are studied using classical three-dimensional (3D) drift-diffusion (DD) simulations. The models for both OTF and LGD are based on transmission electron microscope (TEM) observations. OTF is generated using random roughness steps at SiO_2/Si interface and LGD is generated using random size and position of grains in poly-Si gate. The impact of both models on Vth variation is analyzed by the Takeuchi coefficient, B_{VT}. It is found that both OTF and LGD are not the main origin of Vth variation demonstrated by B_{VT} analyses.

Randomness of discrete fixed charges at SiO_2/Si interface of NMOS, which is thought to be one of the possible origins of threshold voltage (Vth) variation, is investigated using 3D device simulation. Three cases of fixed charge types are assumed; (i) both negative and positive sheet charges exist with zero net charge (mix charges), (ii) only negative sheet charges exist, and (iii) only positive sheet charges exist. B_{VT} is used as a Vth variation indicator. It is found that, even if high concentration of fixed charge (10^{12} cm^{-2}) is assumed, the difference of Vth variation between measured NMOS and random dopant fluctuation model by 3D TCAD still can not be explained, which reveals that other fluctuated parameters exists.

Finally, a new methodology for evaluating dopant profile effect on Vth variability is proposed. Body bias coefficient is a key to the model used in this method. Using this method, pure random dopant fluctuation and its profile effect can be clearly observed.