論文内容の要旨

論文題目

Analog Circuit Technologies for Associative-Processor-Based Recognition Systems

（連想プロセッサに基づく認識システムのためのアナログ回路技術）

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Associative processing or template matching plays an important role in computational scheme in intelligent information processing. Because such a process is computationally very expensive and time-consuming, it would be better if this process is carried out by dedicated VLSI associative processors rather than programs running on a general-purpose computer. Generally, the associative processor is a maximum-likelihood search engine having a huge cache memory for past experience or knowledge and a parallel search architecture. In this thesis, several analog VLSI associative processors have been developed for a variety of purposes of intelligent information processing.

Recently, nanoscale devices have attracted much attention because of its ability in terms of enhanced integration density and ultra low-power consumption. Resonance characteristics are typical inherent non-linear characteristics observed in such devices. There would be a great opportunity for building large scale intelligent systems if we could use such kind of characteristics directly in computation. In addition, as devices at the nanoscale have a higher probability of being defective than conventional CMOS devices, designing reliable circuits with such devices is a major challenge. Thus nanoscale devices are more suitable for building majority-decision-making systems like the operation of associative systems than building logic functions. However, nano devices are still in the research phases, and most demonstrations have been just achieved at the device level or simple circuitry. The work in this dissertation can provide an answer to the question: “How

can we use the exotic non-linear characteristics of nano devices to build computing systems". This is because, in this study, resonance characteristics of these quantum devices were emulated by using a simple NMOS circuitry and utilized to build a large scale system.

Firstly, a single-core associative processor has been developed featuring resonance (or bell-shaped) characteristics and device characteristics variability problem. The key feature in this work is the proposal of a calibration scheme that can mitigate the problem of device mismatches caused by process variations. In addition, the matching cell requires only eight NMOS transistors to implement, enabling a very compact implementation of a matching-cell array. Furthermore, the matching cell can operate in the subthreshold regime which yields an opportunity of very low-power operation. The prototype chip was fabricated using 0.35-μm CMOS technology. The chip operation has been verified by measurement results.

In order to make the system more intelligent by increasing the number of template data, a multi-core/multi-chip scalable architecture has been developed. The system has the possibility of a large database capacity. The global winner is determined by employing a three-stage time-domain winner-take-all (WTA) circuit. Device mismatch problems as well as decision errors associated with inter-chip communication delays have been resolved by introducing a majority-code-decision circuit. Design ideas have been verified by measurement results of the proof-of-concept chip fabricated in a 0.18-μm CMOS technology.

Nonlinear filters, such as MIN, MAX or MEDIAN filters play an important role in image and speech processing. These filters can be implemented by using rank-order filters (ROFs) by setting appropriate rank-order values. In this regard, an analog implementation of rank-order searching circuit for building ROFs has been developed by using a time-domain computation scheme. The architecture can preserve the accuracy of digital implementations but achieves advantages of analog implementations in terms of low-power dissipation and small chip real estate. The searching function is an important operation in associative processing. Thus, such kind of searching circuit mentioned here is applicable to build not only ROFs but also associative processors. The circuit operation has been verified by experimental results obtained from the prototype chip fabricated in a

0.18-μm CMOS technology.

In some applications where we want to search for not only the nearest-match but also an *r*-th nearest-match between the input data and template data, we need functions like in rank-order filters. For this purpose, we have developed an *r*-th nearest-match Hamming distance associative processor inheriting techniques mentioned above. Rank-order searching function is an interesting feature of the proposed architecture, making it different from conventional approaches. The simple configuration achieved in this design comes from the use of only one analog comparator in the rank-order setting circuit for any extension of the number of template words. It enables to combine several rank-order searching circuits in parallel so that a "top-*k*" of nearest matches can be searched for in parallel. Operation of the system is verified by simulation results of the prototype chip designed in a 0.18-μm CMOS technology.

In this study, we address analog circuit technologies and architectures for building associative processors employed in recognition systems, and illustrate those with examples of prototype VLSI chips: a single-core associative processor employing bell-shaped matching cells, a multi-core/multi-chip scalable architecture for large database capacity, a rank-order searching circuit and a Hamming distance associative processor employing time-domain computation techniques. The advantages of low-power operation and high-density integration inherited from analog circuit technologies were demonstrated, which are attractive features to enhance the performance of recognition systems.