論文の内容の要旨

論文題目　Investigations of Carrier Mobility Properties in Multiple Silicon Gate-All-Around Nanowire MOSFETs
（マルチシリコンナノワイヤトランジスタにおけるキャリア移動度特性に関する研究）

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As the size of very large scaling integration (VLSI) scales down into deep sub-micron regime, conventional device scaling concept loses its effect and new physics turn to dominate device performance. Although we have achieved performance enhancement during the device scaling down, it is clear that there is a limit at the end of scaling down and we can not just diminish the device size forever. Accordingly, in ITRS, three different but related concepts are proposed: “More Moore”, “More than Moore”, and “Beyond CMOS”. Until now, we still have no concrete image that what will happened in “Beyond CMOS”, but it is clear that we need to achieve further performance enhancements in Si-based devices before we enter into “Beyond CMOS” era in recent future.

Nanowire is a special structure that owns two-dimensional quantum confinements that plays an important role in “More Moore”. As a promising candidate for future VLSI technology, nanowire has attracted much more and more attention in recent years. Carrier mobility is an important factor that dominates the device transport performance, such as ON current. To understand more details about nanowires transport characteristics and figure out effective methods to obtain performance enhancement, it is necessary to investigate carrier mobility properties in nanowires experimentally. However, for accurate mobility in nanowires, the main difficulty originates from the ultra-small capacitance of one single nanowire, as well as serious parasitic effects within the transport channel. In other words, the intrinsic capacitance of one single nanowire is difficult to be measured directly. Therefore, channel that contains multiple nanowires is necessary. So, how to fabricate multiple uniform nanowires and remove parasitic effects are challenging problems that need to be solved.

The basic objective of this work is to dig out the potential of Si-based nanowire MOSFETs and get further performance gain. To be particular, first of all, we need to propose a special device design to measure nanowire capacitance and achieve experimental mobility data in nanowires; then, one important problem we need to solve is how to remove parasitic resistance and capacitance in order to measure intrinsic mobility in nanowires; finally, based on the information we have obtained on carrier mobility characteristics in nanowires, effective ways on mobility or performance enhancement will be investigated.

In this paper, on the basis of split C-V method together with double L_m method, experimental and theoretical investigations on carrier mobility characteristics in silicon nanowires are described systematically. It is found that side surface orientation plays the key role that determinates the mobility modulation in narrower nanowires, as well as the surface roughness. To be particular, [100]/(100) is the

optimum channel direction for nanowires nMOSFETs while [110]/(110) is the optimum channel direction for nanowires pMOSFETs. In wide nanowires, electron mobility approaches to universal curve in [100]/(100) nanowires while hole mobility approaches to the universal curve in [100]/(110) nanowires due to four identical surrounded surfaces with same orientations. For the same reason (side surface contribution), large mobility degradation is observed in narrower [110]/(100) nanowires nMOSFETs due to the increasing contribution from (110) side surface with low electron mobility, while mobility enhancement is observed in narrower [110]/(110) nanowires nMOSFETs due to the increasing contribution from (100) side surface with high electron mobility. As to [110]/(110) nanowires pMOSFETs, although larger contribution from (100) side surface with low hole mobility exist in narrower nanowires, surprisingly, high hole mobility still can be obtained in high N_{inv}, showing only a little degradation from wide nanowires. This is very impressive since the high N_{inv} region is very important for VLSI applications.

Furthermore, aiming at mobility enhancements, mobility modulations by uniaxial stress is also studied in both nanowire nMOSFETs and nanowire pMOSFETs. In nanowire nMOSFETs, electron mobility enhancement is observed in (110) nanowires and [100]/(100) nanowires by longitude tensile stress. In nanowire pMOSFETs, hole mobility increases by [100] tensile stress while decreases by [110] tensile stress. Since (100) surface has much high sensitivity to [110]-directed stress, if [110] compressive stress is applied, it is believed that large mobility enhancement can be obtained in [110]/(110) nanowires due to the large contribution from (100) side surface.

The results obtained in this thesis give us basic and useful image on carrier transport characteristics, shedding light on the structural optimization of silicon nanowire-based devices in future applications in “More Moore”