論文の内容の要旨

VLSI Circuits and Systems for Directional-Edge-Based Intelligent Image Processing
（方向性エッジ情報に基づく知的画像処理回路・システムに関する研究）

朱　弘博

The continuous progress in semiconductor VLSI technologies during the past several decades has provided the opportunity of realizing *real-time intelligent image processing systems* such as image recognition, object tracking, motion recognition, etc. However, the traditional approach of running image processing algorithms on general purpose processors is not practical for building efficient systems at rational costs with low power-consumption. Therefore, a number of VLSI chips having parallel processing architectures such as graphics processing units (GPUs) have been developed to enhance the performance. Although the processing time can be reduced greatly, such approaches are not still efficient enough due to the complex and expensive image processing algorithms which usually include a number of floating point operations. In order to resolve the problem of such a large gap between the algorithms and their VLSI implementation and to maximally utilize the power of semiconductor technologies, we try to develop algorithms which are compatible with the physical characteristics of VLSI circuits.

The robust nature of the human brain in visual information processing has been attracting a lot of researchers to discover better ways of image processing. Physiology research has revealed that the *directional edge information* in images is utilized as the most important clue in visual object recognition. Being inspired by such a biological principle, a series of *direction-edge-based* VLSI-implementation-adapted intelligent image processing algorithms as well as the corresponding VLSI circuits and systems have been proposed and developed in our laboratory.

This work succeeds the research in such bio-inspired algorithms, circuits, and systems. In order to minimize the latency caused by the image data transfer between the image sensor and the processing circuits, the most serious bottleneck in such systems, digital-pixel-sensor-embedded (DPS-embedded) processors were proposed and designed. The performance of such processor has been verified by building a real-time image recognition system with a very low latency. In addition, a directional-edge-based object tracking algorithm was also proposed and partially implemented in an object tracking system by building processing circuits on FPGAs. In the followings, the work is described in more detail.

Firstly, a DPS-embedded global feature extraction VLSI processor for real-time image recognition has been developed. By combining the block-readout architecture of DSP and parallel processing elements, the latency of local feature extraction has been markedly reduced. By adapting

the rank-order filter algorithm to hardware implementation, global feature extraction is accomplished in only 11 cycles. A prototype chip was designed in a 0.18-μm five-metal CMOS technology. The measurement results show that the VLSI processor can extract features more than 400 times faster than software processing running on a 2-GHz general-purpose processor when operating at 60 MHz.

Then, a DPS-embedded early-visual-processing VLSI processor for real-time intelligent image processing has been developed. Compared with the first chip, the enhancement in the functionality of processing elements in the global image processing block further improves the programmability of the processor. As a result, such a chip can handle multiple algorithms efficiently. A prototype chip was designed in a 65-nm 12-metal CMOS technology. The simulation results show that this VLSI processor can achieve all expected functions.

In order to demonstrate the power of such chips, a real time image recognition system has been developed. The system is based on a VLSI-implementation friendly image recognition algorithm. By using the global directional-edge-feature extraction VLSI processor, the latency between the image capture and the final recognition as small as 906 μs has been demonstrated. The merit of the global feature extraction algorithm that it can focus on more significant features automatically has also been experimentally verified.

In the research on algorithms, a directional-edge-based object tracking algorithm was developed. By using directional-edge-based feature vectors, the system has been made robust against illumination variation. The on-line learning technique and the statistical multiple-candidate-location generation have further improved the performance, making the system robust against object size variation, partial occlusion, and object deformation. The performance was verified by experiments under varying disturbing conditions.

Finally, a simple real time object tracking system based on a restrained version of the prior algorithm has been implemented successfully. By experimental results, this system shows satisfying performance in simple tracking tasks by employing only eight candidate locations. Thanks to the fine-grained VLSI-implementation of the object tracking algorithm implemented in an FPGA, the total processing time for the tracking task has been reduced to about 0.1 ms when the system is running at a frequency of 60 MHz.

In this work, *circuits and systems* for brain-mimicking algorithms have been developed based on a very naive model of the brain. In the algorithms of image processing, *directional edge information* plays an essential role for perception of still images as well as moving images. In these systems, the vast amount of subconscious processing in the mind has been implemented by VLSI chips or FPGAs. In order to build "*real-time responding human-like intelligent systems*" with small hardware volume and low powers, such development of hardware-friendly algorithms and their VLSI implementation in fine-grain parallel architectures are most essential.