論文内容の要旨

論文題目

Analog Feature-Extraction CMOS Vision Sensors for Edge-Based Image Recognition Systems

（エッジ情報に基づく画像認識システムのためのアナログ特徴抽出CMOSビジョンセンサー）

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Real-time image recognition becomes quite important in various applications such as automotive control, robot vision, and so forth. For establishing an intelligent perception system in a power efficient manner, learning from biology and implementing the principle of biological mechanisms is a promising approach. In this reason, a directional edge-based associative processor architecture has been proposed. However, because edge detection is computationally very expensive, software programs running on general-purpose computers are not suitable to real-time and low-power performance. Therefore, it is required to develop dedicated VLSI hardwares for human-like robust image recognition systems.

The purpose of this thesis is developing CMOS vision sensors capable of performing intelligent image processing for human-like perception systems because directional edge detection consumes most part of the computation. For further flexibility of the system, it is necessary to enhance robustness against various kinds of environmental variations. In this point, multiple-resolution image processing in conjunction with the edge-based representation gives scale-invariant robust image perception. On the other hand, thresholding of edge-filtered images is quite important to detect only essential information from the images. In order to make the system compatible to such requirement, further advanced functions need be directly implemented on CMOS vision sensors.

Firstly, multiple-resolution directional edge filtering CMOS vision sensors have been developed for scale-invariant image recognition. A pixel-parallel *self-similitude* computation architecture has been proposed for multiple-resolution kernel convolutions based on focal plane image processing. The *self-similitude* organization has enabled pixel-by-pixel multiple-resolution image filtering with minimal complexity in interconnects. As a result, it has become possible to accomplish any $(1/2)^n$-resolution directional edge filtering in (n+2) steps. Analog proof-of-concept chips using a switched floating-gate MOS technology were designed and fabricated in a 0.35-μm 3-metal CMOS technology, where only the line-parallel processing is carried out by applying the subtraction-separated configuration for enhancing the fill factor. The four-directional edge filtering at full, half, and quarter resolutions was demonstrated by chip measurements.

A non-subtraction configuration of the *self-similitude* image processing architecture has been developed for realizing full pixel-parallel multiple-resolution directional edge filtering. In contrast to the subtraction-separated configuration, subtraction operation has been entirely eliminated from the computation repertory of processing elements in the present configuration. As a result, hardware organization of the multiple-resolution edge filtering CMOS vision sensor has been greatly simplified. In addition, full pixel-parallel *self-similitude* processing has been established without any complexity in interconnects. An analog multiple-resolution directional edge filtering chip implemented using current-mode computation was designed and fabricated in a 0.18-μm 5-metal CMOS technology. The concept has been verified by chip measurements, which show that the four-directional edge filtering at multiple resolutions is accomplished at a rate of 910 frames/sec for 56x56-pixel images.

An edge detection CMOS vision sensor employing global thresholding operation has been developed. A cyclic-line-access computation scheme has enabled seamless directional edge filtering in a row-parallel manner. The global thresholding algorithm adaptively determines the threshold value by taking entire intensity distribution in the image into account and allows us to extract more significant features from input images autonomously. An analog proof-of-concept chip for four-directional edge detection was designed and fabricated in a 0.18-μm single-poly 5-metal CMOS technology. The concept has been experimentally verified by measurements of fabricated chips, where the chips show more than 3.4×10^4 times better performance than that of CPU computation.

In this thesis, we have proved the capability of CMOS vision sensor technologies in conjunction with analog computation, where the vision chips are able to carry out various kinds of advanced image processing. The efficiency is much better than that of the general-purpose processors, and the low-power and real-time computation contributes to performance enhancement of the human-like recognition systems.