論文の内容の要旨

Integrated Phased-Array Photonic Switches for Ultra-Large-Capacity Optical Packet Routing
（超大容量光パケットルーティングのための集積化フェーズアレイ型光スイッチに関する研究）

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The explosive growth of data capacity in communication networks has created new problems to be solved by the research community. The conventional optical-electrical-optical (OEO) networks are suffering from high power consumption. This problem is expected to be more serious in the future because the data capacity is estimated to continue increasing exponentially. Replacing the OEO configuration with transparent optical switching is promising to increase the energy efficiency by avoiding O/E and E/O conversion, (de)multiplexing and bit-by-bit processing. Optical packet switching (OPS) is particularly attractive because it offers the highest network utilization efficiency with bursty traffic.

OPS demands optical components with specifications beyond the state of the art, which makes it difficult to adapt this technology. The optical switch matrix has to reconfigure in time scales of a few nanoseconds or shorter. Moreover, the throughput of the switching fabric in a core OPS node has to be scalable to ultra-high levels approaching or exceeding 1 Pb/s in the near future. The buffer also has to reach sufficient capacity in accordance with the throughput. Optical space switches can be building blocks of both switch matrices and tunable buffers. However, traditional integrated semiconductor switching technologies have difficulties in scaling to ultra-large capacities due to problems including signal quality degradation, footprint, and power consumption.

This dissertation focuses on a novel type of high-speed integrated photonic switch to extend the capacity limit of OPS. This device, referred as phased-array switch, has a number of unique properties. It can theoretically switch to hundreds of output ports in a single stage without cascading; it can switch multi-wavelength signals; and it is completely passive. After a detailed description of the principle of operation of this switch and its design issues, experimental research on this device is presented. The first integrated 1×16 semiconductor photonic switch is among the switches introduced in this section. This device, which demonstrates wavelength dependence less than 0.7 dB in the entire C-band (1530-1565 nm), on-chip loss below 7 dB, average extinction ratio of 18.6 dB, and complete dynamic operation

with a response time of 11 ns (limited by the controlling electronics), has improved the state of the art in integrated semiconductor photonic switching considerably. Another switch exhibits a polarization-dependent loss less than 2.2 dB mostly caused by the polarization dependence of the propagation loss. Moreover, an amplitude-controlled integrated phased-array switch is proposed and investigated theoretically for the first time. This device is capable of switching to an arbitrary combination of output ports simultaneously, i.e. multicasting.

Furthermore, experiments with an OPS node constructed from an all-optical label extractor, a phased-array switch, and an electronic switch controller are presented. There are several OPS demonstrations in the literature, but what makes these experiments special is the demonstration of modulation-format-agnostic routing compatible with wavelength-division multiplexing (WDM). In separate experiments, 160-Gb/s optical time-domain multiplexed (OTDM) on/off keying (OOK) and 120-Gb/s WDM differential phase-shift keying (DPSK) packets have been switched to 16 ports with power penalties below 0.7 dB. The OPS node has operated without manual control throughout the experiments. This OPS node can route packets with arbitrary modulation formats and bit rates as long as they fit in its ultra-broad bandwidth (1 dB bandwidth over 4.5 THz). Especially the modulation format independence is very important since spectrally efficient advanced modulation formats are likely to be used in the future.

An advanced photonic integrated circuit (PIC) consisting of hundreds of monolithic active and passive devices is also reported in this thesis. This fully integrated 1×100 switch fits in a footprint of 6 mm × 6.5 mm including the electrodes. PICs of this type are necessary for low-cost, compact and low-power optical switching; and this PIC shows that phased-array switches have high level of integrability.

Finally, the estimated power consumption of ultra-large-capacity buffered optical packet switching fabrics is studied. Large-scale PICs comprising phased-array switches are assumed to be used for both routing and delay-line-based tunable buffering. The estimated energy per bit consumed by the buffer, switch matrix, switch controller and the semiconductor optical amplifiers to compensate for the optical loss in a hypothetical 1000×1000 router is less than 1.5 pJ/bit. The analysis is based on near-future device characteristics. A router of this scale has a maximum throughput of 1 Pb/s if the payload bit rate is 1 Tb/s per fiber. At this throughput level, phased-array switching is estimated to be 9.4 times as energy-efficient as broadcast-and-select switching, a common transparent switching scheme employed in OPS experiments.

To sum up, this thesis comprises experimental and theoretical research focusing on the application of phased-array switches in ultra-large-capacity OPS nodes. This study, which extends over the borders of device, circuit and subsystem level research, confirms that phased-array switches offer a serious potential for the future OPS networks if a number of technical challenges, mostly related to photonic integration, are overcome.