論文の内容の要旨

Study on Fabrication of (110)-oriented Ge-On-Insulator (GOI) MOSFETs by Ge Condensation Technique and their Electrical Characteristics
(酸化濃縮法を用いた（110）面 Ge-On-Insulator (GOI)MOSFET の作製と
その電気的特性に関する研究)

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Continuous downscaling according to Moore's Law is the driving force behind the development of the high performance Complementary Metal Oxide Semiconductor Field Effect Transistor (CMOS) technology with high speed, low power and high integration density. However, non-conventional device structures and materials compatible with current Si platform are of a great concern as the technical boosters in leading edge, which are known to be appeared in the future generations of traditional Si technology. Especially in the sub-nm region, high attention has been paid to ultrathin-body Si-on-insulator (UTB SOI) structures towards further device scaling. On the othrehand, comparing with the early era of Si technology, nowadays it is a trend to treat the p- and n- type MOSFETs separately to relax the complexity of technical solutions, to constantly increase the performance with downscaling of CMOSFETs in the coming generations. Therefore, in this study, we set our objective to improve the performance of p-type MOSFETs (pMOSFETs) by introducing hole mobility enhancement factors throughout the proposals by channel engineering.

For improving the performance of pMOSFETs, Ge-on-insulator (GOI) structure has been regarded as a promising channel, because Ge provides 4 times higher bulk mobility than Si. Moreover, the enhancement of mobility by choosing the optimal channel direction/surface orientation has already been demonstrated for Si MOSFETs. As for Ge surfaces, simulation based studies have shown that <110> direction of (110) surface orientation is optimal for p channel Ge MOSFETs, because of the lower effective mass. On the other hand, ultra-thin body (UTB) structures on Si substrates are needed for realizing short gate length MOSFETS on the Si platform. One of the promising techniques to fabricate UTB GOI layers is the Ge condensation technique. However, fabrication of UTB (110) GOI layers is still challenging and the device operation of the MOSFETs has not been reported yet.

Towards the possible application as high mobility alternative channels for pMOSFET devices in the era of 22 nm technology node and beyond, the aim of this study is to purpose the combination of three main mobility boosting technologies namely, ultrathin-body GOI structure, <110> channel direction of (110)-crystal orientation and the application of compressive strain to the channel by the viewpoint of channel engineering. In terms of demonstrating the superiority of 12-nm-thick (110)-oriented GOI pMOSFET devices and the physical interpretations to the structural and carrier transport properties, in this study, we have experimentally investigated their characteristics by utilizing the GOI channels fabricated by the Ge condensation technique, mainly focused on the following points.

A.) Characterization of (110)- GOI layers fabricated by the (conventional) Ge condensation technique.

B) Investigation of the effects of annealing in reducing the leakage current of GOI channels.

C) Analyses of the hole mobility dependence on channel direction, effective field and temperature in (110)-GOI surfaces with insights to their physical mechanisms.

D) Application of compressive strain to GOI channels by the local Ge condensation technique and clarify the effect of window size on strain.

First, the epitaxially grown $Si/Si_{0.7}G_{e0.3}$ (40 nm) / (110)-oriented SOI structures as shown in Fig. 1(a) were utilized to fabricate GOI layers by the Ge condensation technique. During this, thermal oxidation was carried out for the initial structure, until the Ge content, confirmed by Raman Spectrometry, was increased up to 100 %.The purity, orientation and strain of the fabricated GOI layers (Fig. 1(b)) were characterized by Secondary Ion Mass Spectroscopy (SIMS), Raman and X-ray Diffraction (XRD) analyses. The presence of the Ge related peaks only in the Raman and the XRD spectra confirms the existence of a pure GOI layer. We have also examined from SIMS measurements that the residual Si content of the GOI layers is less than 0.8 %. The existence of (220) plane reflection in XRD and Transmission Electron Diffraction (TED) measurements have shown the evidences of (110)-Ge orientation. Additionally, it is also found from Raman and XRD measurements that the in-plane compressive strain in the (110) GOI layers is less than 0.1 %, as similar with conventional results, suggesting the negligible impact of strain on mobility.

We have observed high leakage current between Source and Drain and a large positive threshold voltage shift in our GOI pMOSFETs, suggesting a high residual hole concentration which might be attributed to any crystal defects/dislocations or Fermi level pinning at BOX interfaces generated during the Ge condensation technique. As a solution, the effects of thermal annealing (N_2), Forming gas annealing (H_2+N_2) and atomic Hydrogen annealing treatments were carried out to monitor the hydrogen-termination of dandling / active bonds. Their effects were monitored by I_{on}/I_{off} improvement of I_d-V_g characteristics of pseudo-GOI MOSFET structure Fig. 1(c). In order to have a systematic comparison and a better understanding of our results, the relationship between I_{on}/I_{off}^{min} and the annealing temperature is summarized as a parameter of annealing ambient as in Fig. 2. It is clear that the thermal annealing provides almost no improvement on I_{on}/I_{off}^{min} values as it keeps remain in the initial state at each temperature. On the other hand, introduction of hydrogen to the annealing ambient have shown an improvement of I_{on}/I_{off}^{min} up to 450 ˚C. Comparing with forming gas annealing, atomic hydrogen annealing has shown a better improvement at any temperature. This should be due to the fact that the atomic state of hydrogen is chemically more reactive than the molecular state so that the termination by atomic hydrogen happens much easier. If the temperature increases over 450 ˚C, the I_{on}/I_{off}^{min} decreases to the initial level neglecting the presence of hydrogen. However, it can be concluded that the atomic hydrogen annealing at 450 ˚C provides the best improvement of I_{on}/I_{off}^{min} for (110)-GOI surfaces.

For The fabrication of GOI pMOSFETs was carried out by using Pt-Germanide source/drain (Pt-Ge S/D) structure which is known to provide negligibly small series resistance for Ge channels with acceptable thermal budget and the simply the back gate operating structure (Fig. 1(d).In order to examine the hole mobility anisotropy on (110)- and control (100)-oriented GOI pMOSFETs, the angle of the current flow direction of the present devices tilted from <100> direction was varied from 0° to 90° by every 22.5°.

It is found that, the hole mobility on (110)-oriented GOI surfaces increases with the channel direction tilted from <100> to <110> direction, in contrast to (100)-oriented conventional GOI or Si surfaces (Fig. 3). Also it also observed that the E_{eff} dependence of μ_{eff} is different between the (110)- and (100)-oriented GOI or Si surfaces. First, μ_{eff} of the (110)-oriented GOI surfaces ($\square_{eff\text{-}GOI(110)}$) increases with

increasing E_{eff} from low to mid E_{eff} region , while μ_{eff} of the (100)-oriented GOI surfaces ($\mu_{eff\text{-}GOI(100)}$) decreases with increasing E_{eff}. The inversion-layer mobility in low E_{eff} (or N_s) region is known to be subjected to Coulomb scattering. However, D_{it} values of (110)- and (100)-orientated GOI MOS interfaces, which can be regarded as one of the major Coulomb scattering centers, are 1.4×10^{13} cm^{-2} and 0.8×10^{13} cm^{-2}, respectively, extracted from the *S* factors. This small difference of D_{it} is not enough to explain the large difference in the E_{eff} dependence of $\mu_{eff\text{-}GOI(100)}$ and $\mu_{eff\text{-}GOI(110)}$. Furthermore, $\mu_{eff\text{-}GOI(110)}$ keeps increasing with E_{eff} up to mid E_{eff} region, and weakly decreases towards high E_{eff} region. However, $\mu_{eff\text{-}GOI(100)}$ monotonically decreases with E_{eff} up to high E_{eff} region. However, in order to further discuss the scattering mechanism, the discrimination of the mobility components dominating by different scattering mechanisms is necessary.

In order to obtain physical insights into these phenomena, we have extracted phonon-limited mobility of (110)-oriented GOI pMOSFETs through the temperature dependence (Fig. 4). The extracted phonon mobilities on both (100)- and (110)-oriented GOI obey to the dependence of temperature to the power of -1.8, which is similar to the electron and hole mobilities in Si MOSFETs. This finding suggests the dominance of inter-valley phonon scattering. The phonon-limited mobility of (110)-oriented GOI pMOSFETs along <110> is 7.1 time, at maximum, as high as that of (100)-oriented Si pMOSFETs, while that of (100) GOI pMOSFETs is 3.4 times higher.

Figure 5 summarizes the mobility enhancement factor of (100)- and (110)-oriented GOI pMOSFETs, obtained in the present work, as a function of the channel direction angle tilted from <100> direction under different scattering mechanisms in comparison with simulation based results on (100)- and (110)-oriented Ge surfaces. Note that the channel direction dependence of mobility on (110)-GOI pMOSFETs under the each above condition can be confirmed. Furthermore, the origin of the direction dependence of the hole mobility is examined. As a result, the effective mass dependent on the channel direction of (110)-oriented GOI pMOSFETs can be a dominant factor for the observed mobility anisotropy.

Finally, we have carried out the formation of (110)-GOI layers by the local Ge condensation technique in order to accommodate higher amount of compressive strain to the channel as, the conventional Ge condensation technique provides negligible amount of residual strain (around 0.1 %). During the local Ge condensation technique, only a localized area of Si/SiGe/SOI structure defined by window opening of a thick SiO_2 layer capped with the whole sample surface is subjected for Ge condensation, while the other areas preserved in the initial state works effectively to preserve the strain in the localized GOI channel. To clarify impact of the dimensions (L; length and W; width) of the window size on accommodated compressively strain in localized GOI channels, we have systematically changed the window size from 1 um $\times$ 1 um to 700 um $\times$ 300 um and evaluated the average strain inside the each window by Raman spectroscopy as in Fig. 6. It is found that the localized GOI layers up to L=200 um over 1.5 % of strain is preserved with no W dependence, while when the window size reaches to 700 um $\times$ 300 um the compressive strain relaxes to 0.2 % level provided by the conventional Ge condensation technique. However, it can be confirmed that the window sizes up to 300 um $\times$ 100 um, which is compatible with our current device sizes provide over 1.4 % of higher compressive strain, comparing with the conventional Ge condensation technique. These results suggest that the local Ge condensation technique is a practical solution to apply compressive strain to the (110)-oriented Ge pMOSFET along <110> channel direction, as a candidate for high performance MOSFET devices for future generations.

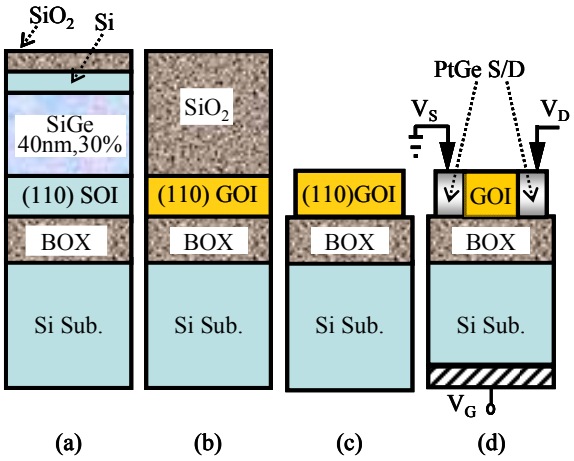

Fig.1. Illustration of fabrication of GOI pMOSFETs

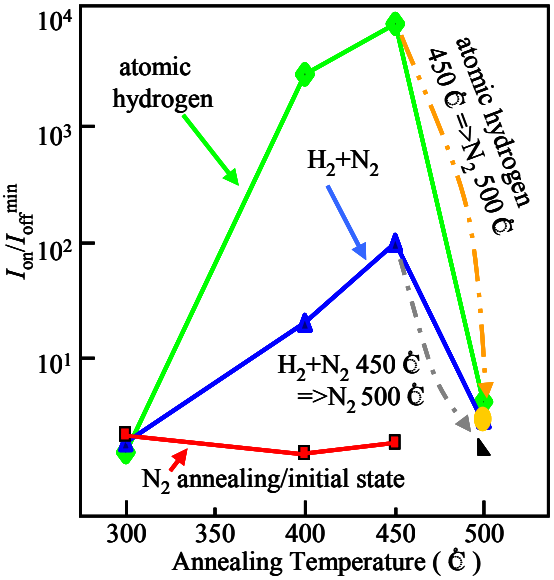

Fig.2 I_{on}/I_{off}^{min} Vs annealing conditions

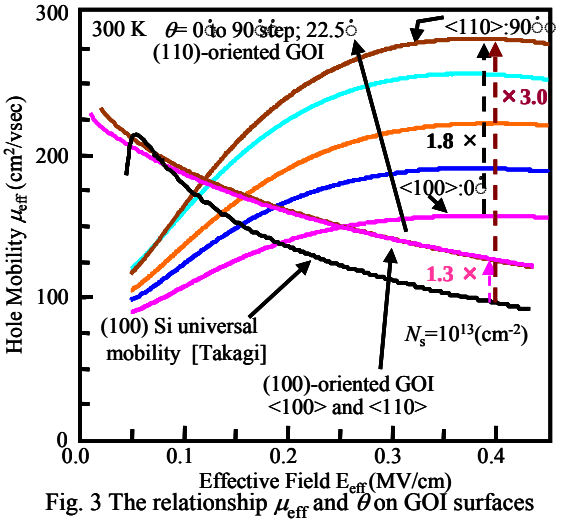

Fig. 3 The relationship μ_{eff} and θ on GOI surfaces

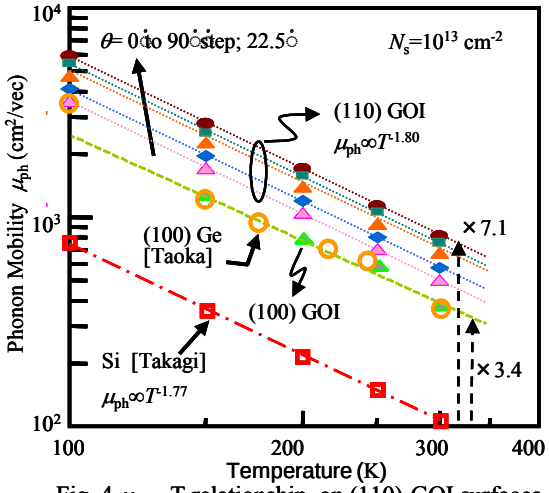

Fig. 4 μ_{ph} - T relationship on (110)-GOI surfaces

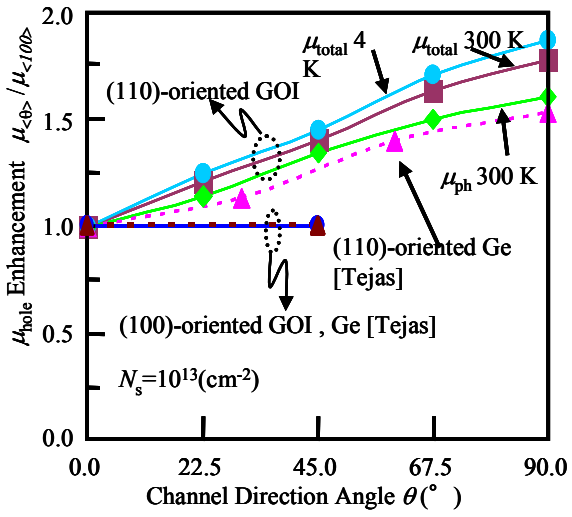

Fig. 5 $\mu_{<\theta>}/\mu_{<100>}$ Vs θ on GOI surfaces

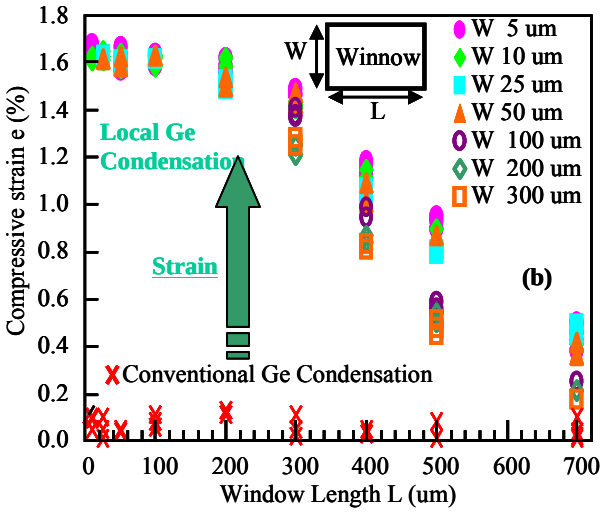

Fig. 6 window size dependence on residual strain