論文内容の要旨

論文題目　　$SrTiO_3$ Heterostructure Field-Effect Transistor Characterization and Process Optimization

（$SrTiO_3$ ヘテロ構造電界効果トランジスタのプロセス最適化と特性）

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Transition metal oxides possess many interesting electronic phases, the stability of which depends on a competition between various forms of charge and spin ordering. Some famous examples are the high-Tc copper oxide superconductors and the colossal magnetoresistance manganites. A common feature of many of these oxide materials is that the appearance of particular electronic phases can be controlled by changing the carrier density and often also the dimensionality. From an applications point of view, it is particularly interesting to look at materials that are close to a phase boundary, as a small change in the environment, for example, temperature, light, or electromagnetic fields, can trigger a phase transition resulting in a large change in physical properties, such as resistivity. This type of behavior can be a basis for new electronic devices for switching, sensing, data storage, etc.

Systematic studies on the effect of small carrier doping changes on the properties of materials are often complicated when traditional chemical impurity doping is used. In this work, a different approach is explored, namely the possibility of modulating the carrier density in a material by electrostatic field effect. This is, of course, what happens in a field-effect transistor and the technique can have a number of advantages; it allows systematic and accurately controlled doping, the doping changes are reversible, and changing the dopant density does not add impurities to the system. It also works best in thin layers, which is the typical geometry for many of the potential microelectronic applications of oxides.

As a model material for the field-effect studies, $SrTiO_3$ was selected as the semiconductor, mostly because it is a convenient choice for thin film growth, but also because the metal-insulator transition occurs in $SrTiO_3$ at a lower carrier density than almost any other oxide.

The work was divided into several stages, with the main effort going into developing the fabrication process of oxide transistor devices. Device performance in oxides is a very complicated issue due to the

need of combining many different materials in an epitaxial heterostructure, while maintaining the expected bulk-like properties. Planar interface-based devices like transistors are particularly sensitive to impurities and defects, usually rapidly degrading the performance of a device and preventing the use of a FET for performing field-effect doping studies.

At first, a process was developed for fabricating epitaxial transistors with a non-doped $SrTiO_3$ channel, a $DyScO_3$ gate insulator, and metallic oxygen-deficient $SrTiO_{3-\delta}$ electrodes. Growth parameters for the insulator layers were optimized to obtain the best interface transport behavior while maintaining low leak currents and high breakdown fields. An unusual feature of the device structure was the use of a double-layer insulator, where the critical channel interface is epitaxial, while most of the gate insulator thickness is provided by an amorphous scandate insulator. A particularly important parameter for managing the transport behavior of the interface and the dielectric behavior of the insulator was the control of the oxygen environment in annealing, film growth, and post-processing stages of device fabrication. It was shown that suitable annealing and deposition conditions at relatively high oxygen pressures are effective in reducing the formation of oxygen vacancies at the critical channel interface. With the help of positron annihilation measurements it was also shown that epitaxial scandate layers can be very convenient oxygen vacancy migration barriers, protecting the device channel. It was found that a fixed charge can easily form in high-k films like amorphous $DyScO_3$. This can impose a field offset on the switching characteristics of transistors.

Many different types of interface structures were tested in the course of this work. The best transistor action and low-temperature operation at low gate fields was obtained by moving away from simple perovskite interfaces to a rock-salt double *A*-site interface consisting of (La,Sr)O. By combining competing tendencies of La to dope carriers into the surface of the substrate and the wide-gap $DyScO_3$ to deplete carriers from the interface, it was possible to obtain high-mobility devices. The atomic structure of the delta-doped FETs was studied by ion scattering spectroscopy, while the potential profiles were probed by hard x-ray photoemission spectroscopy. The conclusion of the work was that it was probably possible to shift the conducting layer away from a defect-rich interface deeper into the substrate.

It is hoped that this work will provide guidance for many further developments in heteroepitaxial oxide device development, particularly in devices that use channel layers with reduced dimensionality and thus larger per-site carrier density modulation levels, making the field-effect approach a truly useful tool for studying the physics of phase transitions in transition-metal oxides.

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