論文の内容の要旨

A Study on Resonant Supply Noise Reduction in Multiple Power Domain LSIs

（多電源ドメイン集積回路における電源共振雑音低減に関する研究）

氏名　　金　鎮明

This dissertation focused on the on-chip resonant supply noise reduction methods to improve signal integrity and reliability in multiple power domain LSIs. Power supply integrity is one of the serious problems in the nanoscale LSIs design. The resonant supply noise generated by the rush current is reported that it has typically 40-200~MHz frequency which is determined by the package inductance and the on-chip capacitance. Long duration and large magnitude of the resonant supply noise, especially the first droop, degrades the circuit performance or causes reliability issues. To make sure the circuit performance and improve signal integrity, power supply noise should be reduced and mitigated. Recently, SoCs have multiple power-domain partitions has been developed and commonly used in low-power LSIs such as SoCs. Because all blocks on a chip rarely work simultaneously, there are some blocks in sleep mode. Each sleep block has a lot of parasitic capacitors such as gate capacitance and junction capacitance. These parasitic capacitors in sleep blocks can be used for reducing the resonant supply noise as an alternative to a large decoupling capacitor.

Chapter 2 presents an on-chip resonant supply noise canceller utilizing active parasitic capacitance of sleep blocks. Recent SoCs have multiple power-domain partitions. Because all blocks on a chip rarely work simultaneously, there are some blocks in sleep mode by turning off the foot transistor. Each sleep block has a lot of parasitic capacitors such as gate capacitance and junction capacitance. These parasitic capacitors in sleep blocks can be used for reducing the resonant supply noise as an alternative to a large decoupling capacitor. The test chip was fabricated in a 0.18um CMOS process and measurement results show 43.3% and 39.8% noise reduction, respectively, when the supply voltage is abruptly changed from 1.8V to 1.4V and vice versa. Also, it achieves 12.5% noise cancelling when a sleeping block is turned on the abrupt wake-up of a sleep block. The proposed method requires 1.5% area overhead for four 100k-gate blocks, which is 7.1X noise reduction efficient comparing with the conventional decap for the same power supply noise, while achieves 47% improvement of settling time.

Chapter 3 presents a decoupling capacitance boosting method for on-chip resonant supply noise reduction for DVS systems. This work utilizes MOSCAPs instead of the parasitic capacitance of sleep blocks for the effective capacitance value boosting. The switching

controls of decoupling capacitors depending on the supply noise states achieve an effective noise reduction and fast settling time simultaneously compared with the conventional passive decoupling capacitors. The proposed method is possible to improve effective capacitance value of the conventional decaps for reducing on-chip supply noise without discharging time even if SoCs do not have multiple power domains. The measurement results of a test chip fabricated in a 0.18um CMOS technology show 12X boost of the effective decap value, and 65.8% supply noise reduction with 96% settling time improvement. Although the proposed method is required more area than previous work, the capacitor boosting effect gets better because of the small well-substrate junction capacitance.

Chapter 4 presents that switched parasitic capacitors of sleep blocks with tri-mode power gating structure to reduce on-chip resonant supply noise. The test chip is implemented in 0.18um CMOS. Body controls of the sleep blocks make it possible to store charge into the parasitic capacitors of sleep blocks due to reduce discharging time for using charge in the parasitic capacitors of sleep blocks. The proposed method achieves 59.6% and 42.7% noise reduction for wake-up noise and 41MHz periodic supply noise, respectively, without discharging time before noise cancelling, and shows a 8.2x boost of effective capacitance value. The area overhead is 2.2% for 500k-gate logic blocks.

Chapter 5 presents that the controlled bridge impedance to reduce the high frequency noise generated by SPC operations. The proposed method can adjust the amount of injected charge into power supply line by controlling the size of bridges. A test chip fabricated in 65nm CMOS achieves 46.9% and 57.9% noise reduction for wake-up noise and 130MHz periodic supply noise, respectively. The proposed method also realizes without discharging time before noise cancelling, and shows a 8.4x boost of effective capacitance value with 2.1% chip area overhead. To apply the proposed switched parasitic capacitors of sleep blocks for reducing resonant supply noise, we can save chip area for noise reduction more effectively.

Now we are sure that these results in this dissertation successfully cancel the on-chip resonant power supply noise generated by the large rush current. It is expected that our research results will make a large contribution to makes more efficient use of the chip area, and improve voltage settling time. As a result, our results will contribute to improve the signal integrity and reliability issues.