論文の内容の要旨

論文題目　CMOS Circuit Building Blocks for Proximity Communication Systems
(非接触通信システムに向けた CMOS 要素回路の研究)

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This thesis focuses on CMOS circuit building blocks for proximity communication systems which are intended for connecting generic low power modules together to form diverse systems which are both low power and have small form factors to fill the cost and performance gap between systems made on boards and custom LSIs.

This thesis is made up of six chapters. The first chapter gives the motivations and goals of this thesis. Proximity communication using inductive coupling and capacitive coupling is a promising way to connect generic low power modules together to form diverse systems. Reconfigurability, high mechanical reliability, low power dissipation, and low implementation cost are some of the significances of proximity communication. A comparison of inductive coupling communication and capacitive coupling communication is given as well as a review of conventional circuits. An overview of this thesis is presented in the final part of this chapter.

Board to board communication using proximity communication can be used instead of conventional mechanical connectors, for high reliability connections in places where vibration or dust can accumulate, while keeping a small footprint. In chapter 2, three types of transceivers for board to board communication are proposed. The first circuit is a capacitive coupling channel with a track and charge scheme. This scheme enables fast reset while eliminating DC leakage paths, allowing the capacitive pads to be exposed, instead of covered with solder mask, enabling the communication distance to be closer and thus reducing the pad size. The second circuit copes with the DC leakage between the transmitter and receiver circuits using capacitors inserted in series with the coupling capacitors. This simple architecture can be used to send clock signals as well as high speed data. Finally, an inductive channel for longer communication distances is explored. One main drawback of inductive channels is the density of inductors that can be placed due to inter-channel crosstalk. This is coped by introducing rectangular inductors. The effect of the

inductor shape on the crosstalk is discussed.

Chip to chip stacking in a package is also a place where proximity communication shows much promise. Conventional proximity channels have shown the potential to connect multiple chips, but LSIs using proximity channels must be separately designed and manufactured since the I/O cannot be shared with conventional bond wire implementation. To overcome this problem, a novel implementation of chip to chip communication using Through Silicon Capacitive Coupling (TSCC) is proposed in chapter 3. TSCC has three features, (1) it allows stacking more than three chips, (2) it enables easy access to the bonding pads for DC power supplies, and (3) it enables the capacitive coupling pads to be used as bonding pads. This allows the I/O to be used for both TSCC and traditional wire bonding, eliminating the need to redesign the chip for both cases. Measurements of chips implemented with TSCC are presented to show the feasibility of this interface.

In low power modules using proximity communication, one of the most power hungry circuit blocks is the clock distribution. In chapter 4, a Switched Resonant Clocking (SRC) scheme is proposed to reduce the power dissipated in the clock distribution. In conventional resonant circuits, when the clock frequency is lower than the designed frequency of the resonant tank, series resonation between the inductor and capacitor inserted to cut DC current occurs and causes large power dissipation and double switching. This makes low speed testing difficult in conventional circuits. This problem is addressed by adding a switch between the inductor and DC cut capacitor, which is turned off at low clock frequencies to prevent series resonance, while reducing the power dissipation in the clock distribution at higher frequencies.

Other circuit blocks to lower the power consumption of proximity communication systems are described in chapter 5. First, post fabrication tuning of logic circuits using gate oxide stress is proposed. This applies high voltage stress selectively on certain gates to relax the inherit mismatch between logic thresholds between gates in logic circuits, thereby lowering the minimum operational voltage of the circuit (VDDMIN). Feasibility of implementing this topology into several different types of logic circuits is explored. Next, a low power voltage reference circuit is proposed. This uses the threshold voltage difference of different types of transistors to make the output voltage. This circuit has a higher output voltage compared to conventional voltage reference using similar topologies. Threshold voltage tuning is also applied here to control the output voltage.

Chapter 6 concludes this thesis.