論文の内容の要旨

論文題目　　Sub-0.5V Extremely Low Power Logic Circuits
（電源電圧0.5V以下の極低電力ロジック回路に関する研究）

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This thesis explores possibility for realization of sub-0.5V extremely low power logic circuits. Transistor variations at low power supply voltage degrade the operation of logic circuits. Thus, the effects of transistor variations are investigated at low V_{DD} and countermeasures against them are proposed in the thesis.

Reduction of power supply voltage (V_{DD}) is an effective method for achieving ultra low power logic circuits since active power is proportional to V_{DD}^2 and leakage power is proportional to V_{DD}. Although circuits exhibit slower speeds at low supply voltage, the trade-off between power and operation frequency remain attractive for energy-constrained systems. Besides, when V_{DD} is near/below the threshold voltage of transistors, logic circuits operate most efficiently. In this way, lowering power supply voltage achieves low power and energy efficient operation. Transistor variations, however, inhibit lowering V_{DD} because the sensitivity of circuits to transistor variations drastically increases under reduced V_{DD}. The main obstacles for low voltage operation of logic circuits are function errors and delay variations of logic circuits, because one function error at a single logic gate is considered as the function error of whole circuits and the delay variations makes the design of logic circuits more difficult at low V_{DD}. These problems must be dealt with properly in design of low voltage logic circuits. Thus, the purpose of the thesis is to reveal the effect of these two problems on logic circuits and propose countermeasures to achieve sub-0.5V extremely low power logic circuits.

At first, function error of logic gates is discussed in 65nm CMOS. Function errors prevent lowering V_{DD} of logic circuits. The minimum operating voltage (V_{DDmin}) is defined as the minimum power supply voltage when the circuits operate without function errors. V_{DDmin} increases with the number of logic gates and CMOS technology down-scaling. Thus, reducing V_{DDmin} of logic circuits is important to achieve extremely low voltage logic circuits. The determinant factors of V_{DDmin} in logic circuits are investigated, and the design criteria to reduce V_{DDmin} are presented. V_{DDmin} consists of $V_{DDmin(SYS)}$ and $V_{DDmin(RAND)}$. $V_{DDmin(RAND)}$ which is random component of V_{DDmin} depends on the random variation of threshold voltage of

transistors and the number of stages of logic gates, while $V_{DDmin(SYS)}$ which is systematic component of V_{DDmin} is determined by the balance of nMOS and pMOS and is minimized when the logic threshold voltage is equal to half V_{DD}. Therefore, $V_{DDmin(RAND)}$ is reduced by increasing width of nMOS and width of pMOS, while $V_{DDmin(SYS)}$ is minimized by optimizing W_P/W_N at a design stage. The body-biasing is effective to compensate for the increase of $V_{DDmin(SYS)}$ due to the die-to-die V_{TH} variation. The optimal body-biasing minimizes $V_{DDmin(SYS)}$ and the forward body biasing decreases $V_{DDmin(RAND)}$. In the measurement, V_{DDmin} is successfully reduced by 45mV from 193mV to 148mV by the forward body biasing.

Next, the effect of delay variations on logic circuits is explored in 65nm CMOS. Delay variations of logic gates make it difficult for logic gate paths to meet timing constraints. If enough setup time margins are considered, operation frequency decreases. By contrast, to meet hold time constraint, hold compensation buffer is inserted into logic gate paths. Therefore, the within-die delay variation dependence on V_{DD} in several types of design under tests (DUT's) is measured with a proposed circuit. The proposed circuit emulates a real logic path because device under tests (DUT's) are inserted between F/F's and F/F-related delays are included in the delay measurement. The main focus of the measurement is dependence of the logic circuits on the methodology of physical layout. Although, Layout of logic circuits is usually designed by automatically using place and route (P&R) tools, the effect of the auto P&R layout on delay variation is not clear at low voltage. Thus, DUT delay dependence on methodology of physical layout is investigated. The measurement result reveals that relative delay variation difference (=sigma/average) between the manual layout and the P&R layout rapidly decreases from 1.56% to 0.07% with reducing V_{DD} from 1.2V to 0.4V, because the random delay variations due to the random transistor variations dominate total delay variations at low V_{DD}. This result indicates that low voltage logic circuits designed by P&R tools do not raise delay variations at low V_{DD}.

Finally, in order to achieve ultra low V_{DD} logic circuits, a post-fabrication dual supply voltage (V_{DD}) control (PDVC) of multiple voltage domains is proposed. Reducing V_{DDmin} at a design phase is difficult because V_{DDmin} is mainly determined by random variations of transistors. Furthermore, only one functional error of logic gates increases V_{DDmin} of a whole logic circuit. Therefore, in order to reduce V_{DDmin}, V_{DD} must be controlled with multiple domains. In the proposed PDVC, the layout of the whole logic circuit is divided into many domains regardless of the functional blocks. The V_{DD} of each domain is independently selected from high V_{DD} (V_{DDH}) and low V_{DD} (V_{DDL}). PDVC is applied to a DES CODEC's circuit fabricated in 65nm CMOS. The layout of DES CODEC's is generated by P&R tools and divided into 64 V_{DD} domains. V_{DDH} or V_{DDL} is applied to each domain and the selection of V_{DD}'s is performed based

on multiple built-in self tests. V_{DDH} is selected in V_{DDmin}-critical domains, while V_{DDL} is selected in V_{DDmin}-non-critical domains. As a result, a maximum 24% power reduction was measured with the proposed PDVC at 300kHz, V_{DDH} =437mV, and V_{DDL}=397mV.

The results of the thesis, which includes investigation on and countermeasures against V_{DDmin} and delay variation, is useful to realize sub-0.5V extremely low power logic circuits for future LSI applications.