論文の内容の要旨
Abstract of Dissertation

# Reaction pathway analysis for dislocation nucleations in Cu and 3C-SiC; A case study on 3C-SiC wafer fabrication process

## (銅と 3C-SiC における転位生成の反応経路解析；3C-SiC のウエーハ製造プロセスにおけるケーススタディ)

孫　瑜

Dislocation nucleation with a critical role on plastic deformation of nano-scale structure has been studied for years, while still remains several unknown features. By means of the atomistic calculation based on reaction pathway analysis, the activation parameters of dislocation nucleation transition have been quantified and some issues have been clarified. However, there is a lack of calculation on dislocation nucleation in binary compounds providing the related minimum energy pathway and saddle-point configurations.

At the more basal point, we start from the calculation of dislocation nucleation in a simple substance Cu, which is a classic fcc crystal. The nucleations of 90° and 30° partial dislocations from a sharp corner in Cu have been investigated. The anisotropy aspects of dislocation nucleation revealed by the results have shown that the stress-dependent activation energy of 30° partial dislocation is approximately twice over the counterpart of 90° partial dislocation, and that the maximum inelastic displacement for the former is also higher. Moreover, the shape of the saddle-point configuration of 30° partial dislocation is similar to a half-ellipse whereas in the case of 90° partial dislocation it is more like a semi-circle, which could be principally ascribed to the Peierls barrier differences between edge and screw components and the inhomogeneous stress field.

To further investigate the dislocation nucleation in binary compounds, 3C-SiC is taken as an example, as a classic zinc blende crystal, moreover as one of the promising semiconductors drawing much attention. By focusing on the core element effect, studies on glide-set 90° partial dislocations with Si-core and C-core nucleated from a sharp corner in 3C-SiC have been carried

out. The results present that both of the stress-dependent activation energy and athermal strain of C-core dislocation nucleation are higher than that of Si-core. Whereas the gradient of the energy curve for C-core nucleation is lower than the counterpart of Si-core, manifesting the greater thermal sensitivity of C-core dislocation. Such results show that the nucleation of Si-core dislocation is more energy-favorable while the C-core dislocation would nucleate with thermal assistance under high temperature, which explicitly explain the previous experiment observation of core nature effects on dislocation performance in SiC. Besides, estimation of dislocation nucleation behavior under high temperature has also been conduced. The free energy is obviously reduced at deposition temperature, implicating the much higher occurrence rate during crystal growth.

In addition, the role of surface step on dislocation nucleation in 3C-SiC has also been revealed. The activation energy required by dislocation nucleation from a surface step is slightly reduced comparing with that from a sharp corner, which demonstrates the facilitative effect of surface step on dislocation nucleation. Discussion on nucleation rate under deposition temperature has been attempted as well, indicating that the temperature could be greatly influential on nucleation criterion.

After the ideal calculation under theoretical level, more realistic technology problems are confronted. The deposition of 3C-SiC on undulant-Si substrate published by Nagasawa and the co-workers is found to efficiently reduce the planar defects and improved crystal quality. However, the saddle-shape warpage of 3C-SiC wafer becomes a problem [1,2]. And the mechanisms of stacking faults formation remain unclear as well. The wafer warpage and poor crystalline quality which are the two main issues hindering the developments and applications of 3C-SiC/Si, are devoted by the following work to provide a reasonable analysis and explanation in some extent.

With the purpose of clarify the causes of wafer warpage, from *ex-situ* curvature

measurements and stress calculation, it is found that large compressive intrinsic stress is generated during high temperature growth (1623 K) in both directions parallel and perpendicular to the ridge of undulation on Si substrate. To investigate the intrinsic stress distribution along the 3C-SiC film thickness, reactive ion etching (RIE) has been performed on 3C-SiC film to determine the dependence of SiC/Si system curvature on the remained 3C-SiC thickness. Then, by analyzing the experiment data, it is reflected that intrinsic stress component perpendicular to the ridge of undulation shows nonuniform distribution along the film thickness. Below the 50 μm thickness region, the distribution presents large variation. To explain the warpage in a quantitative manner, the calculation by finite element method taking the intrinsic stress distribution as input has been performed and the obtained curvature of 3C-SiC wafer is in agreement with experiment data. Besides, the obtained intrinsic stress distribution shows very similar distribution of stacking faults, which displays high density near SiC/Si interface and rapidly decreases within 50 μm thickness. It is speculated that the microstructure changes induced by the stacking fault reduction process (stacking fault collision) would be the cause of the intrinsic stress variation.

Moreover, from the viewpoint on glide behavior of partial dislocations as the boundary of stacking faults, the distinct performances involving expanding or shrinking of stacking faults with Si-face ($SF_{Si}$) and C-face ($SF_C$) exposing on (001) surface observed by Nagasawa have been deliberated. By the perspective of dislocation mobility, it is thought that the $SF_{Si}$ bounded by two Si-core 30° partials or one Si-core 90° partial and one C-core 30° partial should be expanding during crystal growth. Whereas, the $SF_C$ sandwiched by two C-core 30° partials should be shrinking, which gives rise to the reduction of $SF_C$ having no relation with undulation on Si substrate. While the other kind of $SF_C$ contains one C-core 90° partial and one Si-core 30° partial as two sides tends to extend itself. Such one could be reduced with the help of enhanced stacking faults collisions due to the undulant-Si substrate. Consequently, it is supposed that the reduction of stacking faults is attained not only thanks to undulation on Si substrate but also because of the different characters of the bounding partial dislocations, which could be

instructive for the controlling of stacking faults and improvement of 3C-SiC crystal quality.

The calculations and proposals have mainly promoted the understanding on mechanisms of dislocation formation in 3C-SiC at both theoretical and technological level, which may supply possibility to the further progress of binary semiconductors.

References

[1] H. Nagasawa, K. Yagi, T. Kawahara and N. Hatta, Chemical Vapor Deposition 12 122-124 (2006).

[2] H. Nagasawa, M. Abe, K. Yagi, T. Kawahara and N. Hatta, Physica Status Solidi (b) 245(7) 1272-1280 (2008).