論文の内容の要旨

論文題目　A Study of Carrier Mobility and Variability in Silicon Nanowire MOSFETs
（シリコンナノワイヤ MOSFET におけるキャリア移動度と特性ばらつきに関する研究）

氏名　毛　珂

In the past several decades, the size of a metal-oxide-semiconductor field-effect-transistor (MOSFET), the basic element in very-large-scale integrated circuits (VLSI), has been scaled down for higher integration and higher performance. As of 2012, the gate length of MOSFETs has reached a sub-30 nm regime. However, as the scaling proceeds, several problems stand out and prevent more miniaturization of MOSFETs.Among all the issues arise to handicap the continuous device scaling, two issues are with most great importance, one is the short channel effect (SCE), and the other is the variability.

To curb the short channel effect, devices with multiple gates have been developed to improve the gate-channel controllability for better electrical characteristics with the progress in nano-scale fabrication technology. Among all the promising post-CMOS structures, the Silicon nanowire MOSFETs, have attracted much attention with their high immunity to short-channel effect for a promising candidates for future VLSI technologies with high performance in recent year. In actual applications, we care about the devices performance, such as ON/OFF drive current and operation speed; however, the underlying physical mechanism is the carrier mobility in the transport channel. Most of the experimental works on mobility in silicon nanowires are carried on with either indirect extraction method or special structure (for example, multiple nanowire array) to circumvent the difficulty originated from the ultra-small size of the silicon nanowire. The intrinsic carrier mobility of single nanowire is still in the dark.

Along with the rapid device scaling, the variability turns to be one of the critical concerns. Threshold voltage (VTH) variability considerably degrades the stability of integrated circuits. The minimum operation voltage (Vmin) in logic circuits is limited by device variability, and static random access memory (SRAM) fails at a low supply voltage owing to transistor unbalance in a cell. It is now mandatory to take this variability into consideration in circuit design to maintain a high yield. It is known that random dopant fluctuation (RDF) is the dominant origin of random VTH variability in conventional bulk MOSFETs. Recently, it is reported that the variability of both DIBL (drain induced barrier lowering) and COV (current-on-set voltage) is also caused by RDF and leads to instability of SRAM cells and drain-current variability. It is shown that intrinsic channel fully depleted (FD) silicon-on-insulator (SOI)

MOSFETs have not only a smaller VTH variability but also smaller DIBL and COV variabilities owing to the absence of RDF. However, the DIBL and COV variabilities still remain, possibly owing to the variability of workfunction in the metal gate electrode, and further reduction of variability is strongly required for better circuit performance variability and SRAM stability. The variability in silicon nanowire MOSFETs should be studied to investigate the variability mechanism for the possibility of further variability suppression.

The purpose of this work is to evaluate the potential of silicon nanowire MOSFETs for promising “More Moore” device in terms of both device performance enhancement and stability improvement. In this work, silicon nanowire FETs with various designs are extensively studied for carrier mobility and variability. This work is based mainly on the experiments including device design, sample fabrication and characteristic measurement.

In this paper, on the base of split C-V method, experimental and theoretical investigations of carrier mobility characteristics in single silicon nanowires are described systematically for the first time. It is found that side surface orientation plays the key role that determinates the mobility modulation in narrower nanowires, as well as the surface roughness.

And, it is experimentally found that within-device variability of not only VTH but also those of DIBL and COV is suppressed in intrinsic channel nanowire FETs owing to the non intentionally doped channel and the absence of gate workfunction variability. The intrinsic channel silicon nanowire MOSFET is promising for a future scaled device structure in terms of not only the short channel effect suppression but also the variability suppression.