論文の内容の要旨

論文題目　Formation of Ge Gate Stack Structures by Plasma Post Oxidation and Their Applications to Ge CMOS Devices
（プラズマ後酸化によるGeゲートスタック構造の形成とGe CMOS素子への応用）

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Recently it is becoming increasing difficult to further improve the performance of Si MOSFETs, because the conventional device scaling is approaching its physical limit. Therefore, the Ge is considered as one the most promising channel materials serving in future CMOS devices due to its high bulk electron and hole mobility. For revealing high performance Ge CMOS devices, advanced high-*k*/Ge gate stacks with both thin EOT and low D_{it} are mandatory. In this research, we focus on the fabrication technique for the Ge gate stacks with thin EOT and high quality MOS interfaces simultaneously. The Ge CMOS devices with these thin EOT and low D_{it} gate stacks are also demonstrated.

First, the drawback of the conventional fabrication technique, which is depositing high-k after the IL formation, is examined by applying an ALD Al_2O_3 on GeO_2/Ge structures. It is found that the GeO_2/Ge MOS interface degrades significantly with decreasing the GeO_2 IL thickness to 1.5 nm, due to the damages induced by high-k deposition. We found that although the GeON/Ge MOS interfaces formed by an *in-situ* plasma nitridation of GeO_2/Ge structures exhibit stability, the EOT scaling is still limited by the difficulty in growing ultrathin GeO_2 layers and the degraded GeON/Ge MOS interface attributed to N cooperation. By optimizing the GeON thickness and N content, an thinnest EOT of 2.2 nm and a relatively low D_{it} of $4\sim5\times10^{11}$ $cm^{-2}eV^{-1}$ have been revealed using an Al_2O_3 (2 nm)/GeON (1.5 nm)/Ge gate stack with a N/Ge ratio of 0.34 in the GeON IL, indicating the intrinsic EOT scaling limit with maintaining a superior MOS interface using a conventional process.

In order to overcome the limit of conventional fabrication process, a plasma post oxidation methodology has been purposed to form a GeO_x IL beneath an Al_2O_3 capping layer by exposing oxygen assisted electron cyclotron resonance (ECR) plasma to a thin ALD Al_2O_3/Ge structure. Here the GeO_x IL is free of the high-k formation induced damages. In addition, the Al_2O_3 capping layer serves as a protection to the thin GeO_x IL against the harmful species in the atmosphere. The low temperature during the plasma post oxidation can also prevent the thermal damage to thin GeO_x/Ge interfaces. The structure and chemical components of these Al_2O_3/GeO_x/Ge structures are analyzed in detail. It has been confirmed that by

adjusting the Al_2O_3 capping layer thickness and plasma condition, the thickness of GeO_x IL can be precisely controlled down to 0.3 nm. The growth behavior of the GeO_x ILs has been investigated using both Ge (100) and (111) substrates. It is observed by both X-ray photoelectron spectroscopy (XPS) and transmission electron microscopy (TEM) that the GeO_x/Ge interface formed by a 300 ℃ plasma post oxidation exhibits relatively large interface roughness. In contrast, the GeO_x IL evolutes layer-by-layer atomically with a room temperature plasma post oxidation, yielding a atomic flat GeO_x/Ge interface.

The electrical properties of the Al_2O_3/GeO_x/Ge gate stacks formed by plasma post oxidation have been investigated systematically. Through the comparison of the MOS interface qualities of Al/Al_2O_3/GeO_x/Ge MOS capacitors fabricated by a conventional procedure and the plasma post oxidation method, it is confirmed that the plasma post oxidation shows significant advantage in revealing a lower D_{it} under a thinner EOT. The properties of GeO_x/Ge MOS interfaces fabricated with various conditions are characterized. It is found that the plasma power, the post oxidation time and the Al_2O_3 thickness do not affect the GeO_x/Ge MOS interface quality. The GeO_x IL thickness is the dominating factor of the D_{it} and it is confirmed that a GeO_x IL as thin as 0.5 nm is sufficient to suppress the D_{it} at the GeO_x/Ge interface. This thickness of GeO_x corresponds to the EOT of 0.35 nm, indicating the feasibility of further EOT scaling of low D_{it} Ge gate stacks using the plasma post oxidation methodology. From the view point of chemical components of GeO_x ILs with different thicknesses, it is interestingly found that the complete oxidation state (GeO2) is not necessarily needed to guarantee a low D_{it}, which is a complement to previous theory. With an optimization of the Al_2O_3/GeO_x/Ge gate stack structure and the plasma conditions, a sub-nm EOT of 0.98 nm has been realized with a low D_{it} in the 10^{11} $cm^{-2}eV^{-1}$ order.

The Ge p- and n-MOSFETs have been realized using the Al_2O_3/GeO_x/Ge gate stacks formed by plasma post oxidation. The record high hole of 401 cm^2/Vs and electron mobility of 693 cm^2/Vs are achieved at a sub-EOT of 0.98 nm for the (100) Ge p- and n-MOSFETs, respectively. The impact of the EOT scaling has been investigated for these Ge p- and n-MOSFETs and it is found that the hole and electron mobility of Ge p- and nMOSFETs can still be improved by reducing the column scattering center at the MOS interface even at an EOT region of ~1 nm. Also, it is confirmed that the rapidly increase of slow traps near the conduction band edge of Ge causes stronger degradation of Ge nMOSFETs with scaled EOT. Therefore, sufficient passivation of these slow traps would be another booster to further improve the performance of Ge nMOSFETs. By revealing an atomic flat GeO_x/Ge interface through a room temperature plasma post oxidation, it is also found that the high field mobility of the Ge p- and n-MOSFETs improve around 20% and 25% at N_s=10^{13} cm^{-2}, compared with the Ge p- and n-MOSFETs with a normal GeO_x/Ge interface fabricated by 300 ℃ plasma post oxidation. By comparing with the results in previous reports, it is confirmed that the mobility degradation with EOT scaling can be sufficiently suppressed with the superior MOS interface passivation by present Al_2O_3/GeO_x/Ge gate stacks. For the (100) Ge pMOSFETs, an improvement

of 80% has been revealed compared with previous reports with a comparable EOT of 0.98 nm. For (100) Ge nMOSFETs, current Ge nMOSFETs exhibits a 3.1 times higher peak mobility than that reported in previous researches under an EOT of 1.2 nm.

In order to further scale down the EOT of Ge gate stacks beyond 1 nm, the plasma post oxidation method is also extended to HfO_2 based Ge gate stacks. However, during the plasma post oxidation of HfO_2/Ge structures, a uniform $Hf_xGe_yO_z$ layer with a poor $Hf_xGe_yO_z$/Ge interface is formed rather than an HfO_2/GeO_x structure due to the strong atom pumping property of HfO_2. In this research, an Al_2O_3 diffusion control layer (DCL) is introduced between the HfO_2 and Ge to suppress the inter-mixing between HfO_2 and GeO_x during the plasma post oxidation. It is found that 0.2 nm is the minimum thickness for the Al_2O_3 DCL to sufficiently prevent the HfO_2-GeO_x inter-mixing and form a high quality GeO_x/Ge MOS interface. By changing the plasma post oxidation time, it is confirmed that the formation GeO_x IL is the key to reveal a low D_{it} in this HfO_2 based gate stack. Especially, with the help of 0.2-nm-thick Al_2O_3 DCL, an EOT of 0.76 nm and a D_{it} of 2×10^{11} $cm^{-2}eV^{-1}$ have been realized for the HfO_2 (2.2 nm)/Al_2O_3/Ge structures after a room temperature plasma post oxidation, where a 0.35-nm-thick GeO_x IL is formed.

The (100) Ge p- and n-MOSFETs have also been fabricated using the $HfO_2/Al_2O_3/GeO_x$/Ge gate stacks having 2.2-nm-thick HfO2, 0.2-nm-thick Al_2O_3 and different plasma post oxidation time. By combining the low D_{it} GeO_x/Ge MOS interfaces formed using an Al_2O_3 DCL and an atomic flatness for the GeO_x/Ge interface revealed by room temperature plasma post oxidation, both high peak mobility and high field mobility is realized for the $HfO_2/Al_2O_3/GeO_x$/Ge p- and n-MOSFETs which is comparable or even higher than those in Ge MOSFETs with thick (~20 nm) GeO_2/Ge gate stacks, under an EOT of 0.7~0.8 nm. Especially, record high hole mobility of 596 and 546 cm^2/Vs have been realized under EOT of 0.82 and 0.76 nm for the $HfO_2/Al_2O_3/GeO_x$/Ge pMOSFETs. For the Ge nMOSFETs, the peak electron mobility of 690 and 754 cm^2/Vs are achieved using the $HfO_2/Al_2O_3/GeO_x$/Ge gate stacks having EOT of 0.76 and 0.82 nm. Compared with the reported data, a 5.1 times improvement of peak hole mobility is realized for the (100) Ge pMOSFETs with present $HfO_2/Al_2O_3/GeO_x$/Ge gate stack under a similar EOT of 0.8 nm. For the Ge nMOSFETs, this research demonstrates the thinnest EOT ever reported in the world.

This research systematically investigated the properties of thin EOT Ge gate stacks. A plasma post oxidation methodology has been purposed to fabricate the GeO_x IL in thin EOT and high quality Ge gate stacks. The properties of thin GeO_x/Ge interface have been investigated in detail. The high mobility Ge CMOS devices are also demonstrated using the plasma post oxidation Al_2O_3/GeO_x/Ge and $HfO_2/Al_2O_3/GeO_x$/Ge gate stacks with sub-EOT. This research indicates the feasibility of the plasma post oxidation technique in future scaled CMOS technology.