論文の内容の要旨

Abstract of Dissertation

論文題目

First principles analysis of materials properties modification at heterointerfaces

（異相界面における物性変調の第一原理解析）

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1 Introduction

Recent advances in fabrication and evaluation techniques have made possible the design and evaluation of devices at the nanometer or even sub-nanometer scales. Such devices sometimes exhibit peculiar properties that cannot be explained by the bulk properties of the constituent materials. This is presumably due to the modulation of materials properties at interfaces, which becomes significant with increasing interface to bulk ratios in nanodevices. Furthermore, such interface effects are not limited to nanodevices; the properties of a bulk material can also be altered through the introduction of a sufficient density of interfaces. Thus, the control and active utilization of such interface properties represent an entirely new degree of freedom in materials and device design. However, the origins of such interface effects are still unclear in many cases, and design principles for utilization of such effects are in dire need. In this dissertation, we tackle this issue by first principles materials modeling. We present analyses of the mechanisms for modification of dielectric response and ion transport at interfaces. We also propose ideas for controlling those effects for obtaining the desired properties.

2 Ionic space charge layer at metal/oxide interfaces

In bulk materials, the charge neutrality condition must be fulfilled because otherwise, the electrostatic potential would diverge. However, at interfaces, this is not the case; in general, a thin charged layer is formed to keep the electrochemical potential constant across the interface. This space charge layer can consist of the deficiency or excess of various ionic and/or electronic carriers, which can lead to modification of electrical conductivity. However, few works have dealt with the space charge formation at metal/ionic conductor interfaces despite their increasing importance in the development of electrochemical devices such as solid oxide fuel cells. To simulate the space charge effect at such interfaces, we took a combined ab initio and continuum modeling approach. In this scheme, the relation between defect concentration and the local potential is first obtained from first principles. This relation is then used to construct a continuum model for simulating space charge profiles at various atmospheric conditions [1, 2].

Figure 1 shows the simulation results for the oxygen vacancy concentration and valence band profiles in acceptor-doped zirconia adjacent to an interface with metal (oxygen vacancies are the dominant charge carriers in this system). It is found that oxidizing atmosphere and high valence band offset result in vacancy depletion, while the opposite trend is seen in reducing atmosphere and low valence band offset. The space charge region is confined to within 2 nm from the interface. This can be understand in a similar manner to space charge formation at metal/semiconductor Schottky junctions: ionic space charge is accumulated at the interface to align the Fermi levels in the metal and ionic conductor, just like electrons or holes are accumulated to align the Fermi levels at metal/semiconductor interfaces. The important difference is that the Fermi level in an oxide can be controlled within a rather wide range by the oxygen atmosphere. The Fermi level position is higher in the band gap in reducing atmosphere compared to oxidizing atmosphere ($\Delta E_{\mathrm{F,bulk}}$ in Fig. 1).

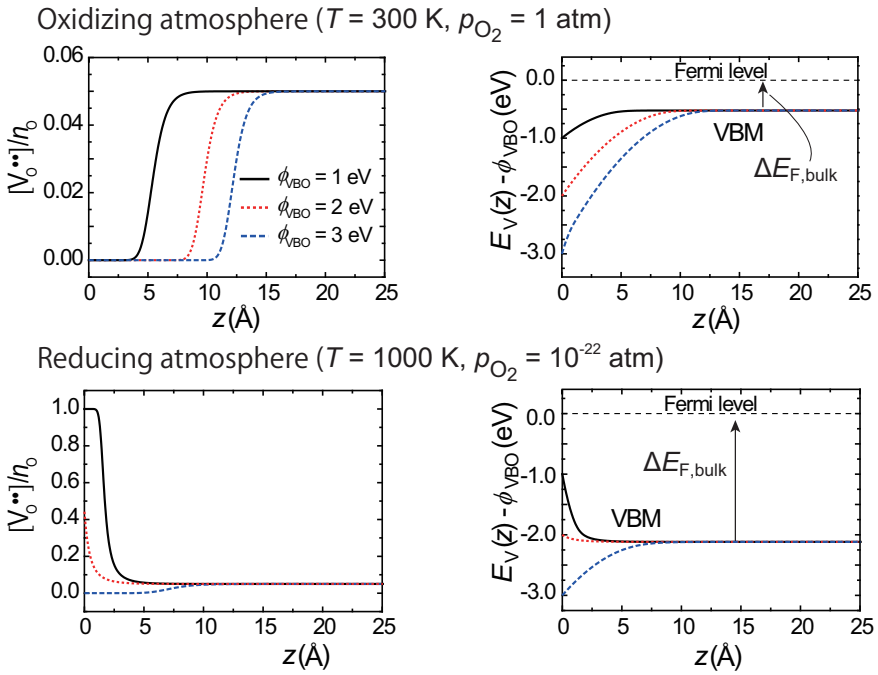

Fig. 1 Oxygen vacancy concentration and valence band maximum (VBM) profiles calculated in an oxidizing atmosphere (top) and a reducing atmosphere (bottom) for various values of the valence band offset(ϕ_{VBO}). The interface with metal is located at $z = 0$.

3 Orbital separation approach for simulating metal-insulator-metal capacitors under bias voltage

The capacitance is a fundamental variable in the design and operation of devices such as transistors and capacitors. As the dielectric layer is made thinner in order to keep up with Moore's law, it has been found that the capacitance often deviates from the classical geometric capacitance $C = \epsilon S/d$, where ϵ is the bulk dielectric constant, d is the dielectric thickness, and S is the area of the electrode plates. This is presumed to be due to the property of the metal-dielectric interface, whose impact on the overall capacitance becomes larger with increased interface to bulk ratios. Furthermore, it has been pointed out that the total capacitance includes contributions of quantum mechanical origin, which becomes significant as the geometric capacitance becomes larger as $d \to 0$.

First principles simulation based on the Kohn-Sham (KS) formalism of density functional theory is a powerful tool for examining such effects. However, the calculation of capacitance requires the application of bias voltage on a metal/insulator/metal (MIM) structure, and this is incompatible with the conventional KS scheme which seeks the global ground state. Although several methods have been proposed to circumvent this problem, they have not seen widespread use due to problems in accuracy and/or efficiency, geometric constraints, and difficulty in implementation.

To rectify this situation, we propose a new method that is based on the separation of the KS orbitals near the Fermi level into each electrode (Fig. 2). The separated orbitals are occupied according to different Fermi levels, allowing for consideration of bias voltage in a straightforward manner. We refer to this method as the *orbital separation approach* (OSA) [3].

The OSA was implemented in Vienna ab initio Simulation Package, which is a widely-used code for first principles electronic structure calculations. We then tested this method by performing calculations of the capacitance and dielectric response in Au-vacuum-Au, Au-MgO-Au, and graphene-vacuum-graphene capacitors, and demonstrated that the method is robust, efficient, and reliable. This method is used extensively in the following chapter to examine the modulation in dielectric response at metal/high-k oxide interfaces.

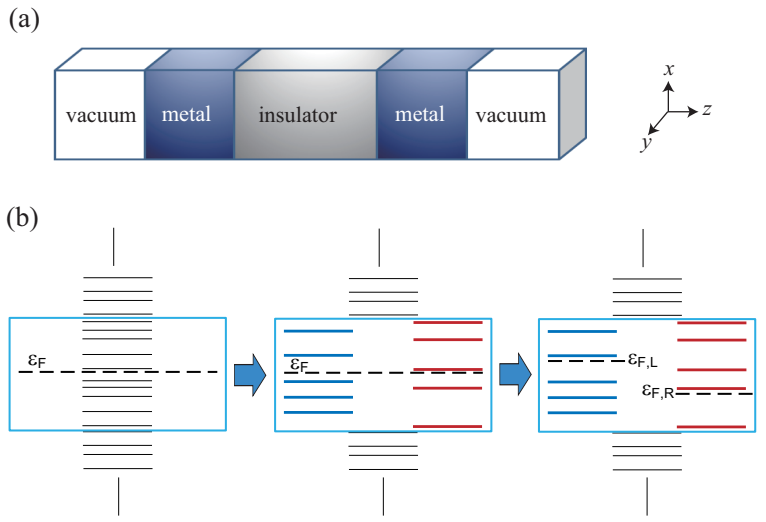

Fig. 2 (a) Schematic of the MIM slab structure simulated in this study. The box indicates the boundaries of the periodic boundary condition employed in the calculations. (b) Schematic of the orbital separation procedure within a preset window around the Fermi level.

4 Countering the intrinsic dead layer effect utilizing ferroelectric negative capacitance

The use of higher-k dielectrics such as $SrTiO_3$ and TiO_2 is being explored for further increase in capacitance density, particularly for dynamic random access memory applications. When using these materials in thin-film geometries, however, it has been found that the capacitance is reduced significantly from nominal values (i.e., those calculated assuming that the dielectric constant is the same as in bulk). First principles simulation have shown that a large part of this reduction can be explained by an "intrinsic dead layer effect" [4]. That is, the dielectric response at interfaces is reduced significantly compared to the bulk, even when the interface is atomically sharp with no defects or interdiffusion. Thus, we need to go beyond the conventional wisdom of simply using thinner dielectrics with higher dielectric constant to increase the capacitance further.

One approach to enhancing capacitance is through the use of negative capacitance. A negative capacitor is thermodynamically unstable, but can be stabilized by placing in series with a positive capacitor. Recently, the idea of placing a ferroelectric in series with a paraelectric for negative capacitance stabilization was proposed and then demonstrated experimentally on ferroelectric/paraelectric bilayer structures [5]. However, the effect was seen only at elevated temperatures over 300° C, limiting its usefulness for device applications. In this work, we consider the possibility of using ultra-thin ferroelectric film to counter the dead layer effect at realistic operating temperatures.

Figure 3 shows the inverse permittivity profile in the $SrRuO_3/SrTiO_3/SrRuO_3$ (SRO/STO/SRO) capacitor calculated using the orbital separation approach (OSA). A clear drop in the permittivity is observed at the interface, reconfirming the dead layer effect mentioned earlier. The calculated capacitance is only 20% of the nominal capacitance, verifying the extremely deleterious effect of the interface on the capacitance of nanocapacitors. We then sandwiched 3 layers of ferroelectric $BaTiO_3$ (BTO) between SRO and STO. The calculated permittivity profile of this system (Fig. 4) clearly shows that the interfacial dead layer is countered by the negative capacitance of the ultra-thin BTO film. The capacitance is 70% (40%) larger than the SRO/STO/SRO capacitor when negative (positive) bias is applied. We also note that the BTO ultra-thin film is centrosymmetric, i.e., the spontaneous polarization is suppressed. The suppression of polarization is, in fact, the prerequisite for ferroelectric negative capacitance [6].

The above results suggest that the utilization of ferroelectric negative capacitance is a viable approach for capacitance enhancement, especially in view of the problematic intrinsic dead layer. The calculations performed are essentially 0 K simulations, so we expect that this effect will be seen at room temperature, rather than at 300° C reported in the experiment on thicker ferroelectric films [5]. Although we carried out calculations on capacitors with ultra-thin dielectric films (up to just a few nanometers), the cancellation of the dead layer has implications for much thicker capacitors. This is illustrated by the fact that according to our results for the interfacial capacitance, even a 54-nm thick SRO/STO/SRO capacitor is predicted to have only 74% of nominal capacitance due to the intrinsic dead layer (such significant impact of the dead layer on the total capacitance was also pointed out in Ref. [4]). Thus, the dead layer cancellation by just three unit cells of BTO at the interface can be expected to enhance the capacitance of capacitors that are much thicker

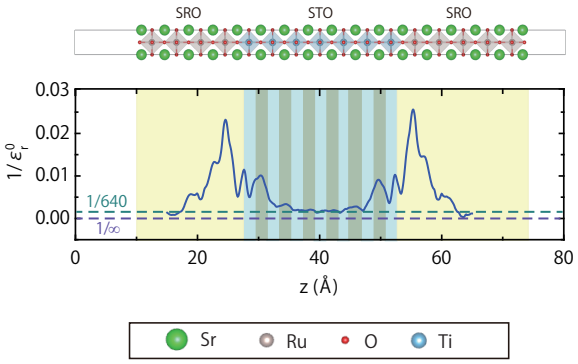

Fig. 3 The calculated inverse permittivity profile of the SRO/STO/SRO capacitor.

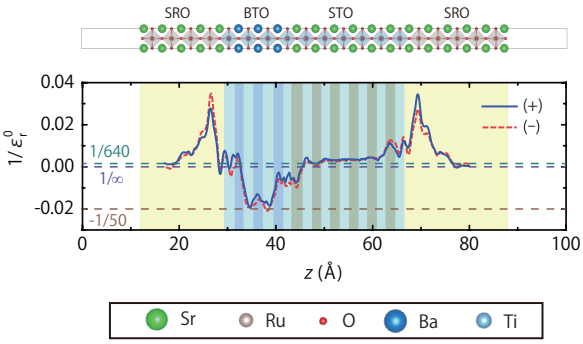

Fig. 4 The calculated inverse permittivity profile of the SRO/BTO/STO/SRO capacitor when positive (+) and negative (-) bias is applied on the right electrode.

than those explicitly considered in the present simulations.

5 Ferroelectric domain formation in thin-film geometries

We pointed out above that the suppression of spontaneous polarization is required for a ferroelectric to exhibit negative capacitance, and that this is realized for ultra-thin BTO sandwiched between SRO and STO. However, the above calculations only considered the monodomain situation, while it has been pointed out that even for very thin films, polar distortion can occur by forming 180° striped domains with the polarization pointing in the out-of-plane direction [7]. If polar distortion occurs, the negative capacitance will not be realized. The literature indicates that domain formation or its suppression depends on the boundary condition and the specific materials, and no general criteria for spontaneous polarization in ultra-thin films have been found.

To help clarify this issue, we performed structural optimization of domain structures in ferroelectric thin films to see if spontaneous polarization is stable in various geometries. When considering $PbTiO_3$ in place of $BaTiO_3$ in the capacitor geometry mentioned above, polarized domains are clearly observed. In contrast, the polarization of $BaTiO_3$ is suppressed in the same geometry, although it is not completely zero as in the monodomain calculation. It is possible that finite temperature effects will reduce the polarization further, although we have not been able to carry out such calculations at the moment.

6 Summary and outlook

We simulated the modulation of ionic carrier concentration and dielectric response at interfaces, and suggested recipes for controlling those properties. The understanding obtained here should be helpful in designing new materials through the active utilization of interfaces that provide better performance or reliability compared to conventional materials. It may even be possible to fabricate materials with novel functionalities. However, ion concentration and dielectric response are semi-static properties of materials. Future works on the *dynamics* of interfaces should have even more impact on the design of interfaces for high performance, reliability, and novel functionalities. We expect that the methodologies and ideas developed in this dissertation will be instrumental in the future research in that direction.

References

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