論文の内容の要旨
Abstract of Dissertation

論文題目　A Study on Low Power VLSI Design using Fine Grained Leakage Control
(細粒度リーク制御による低電力VLSI回路設計に関する研究)

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Since process technology has been in the deep sub-micron era, leakage power reduction is one of the major concerns in modern VLSI circuit design.

Power Gating and Body Biasing are promising techniques for leakage saving and are commonly used in products from low-end micro-controllers to high performance server processors. Recently, leakage power becomes non-negligible compared to dynamic power not only standby block but also running blocks because of process technology scaling and low threshold voltages to achieve higher performance.

However, their leakage saving opportunities are confined to standby-time with whole chip granularities or Run-time with coarse granularities, such as processor core or IP macro level.

To achieve further leakage saving, approaches which introduce finer sleep granularities, e.g. functional unit level, and save leakage power even in run-time are studied.
Introducing finer grained control is able to achieve leakage saving even in running core, however, there are difficult problem to realize fine grained control.

One is area overhead for applying PG structure. For PG circuit, introducing finer control granularity is expected to incur severe area increasing situation for sleep transistor insertion. Therefore, we introduced a novel sleep transistor sizing method for module-based PG circuit to relax that situation by solving the optimal size which meets necessary and sufficient condition.

Evaluation results shows that our sleep transistor sizing reduces average sleep transistor are by 40¥% compared to previous work. Also it produces more desirable sleep transistor width than previous work and reduces 36.7¥% of error between the given performance constraint and actual circuit delay.

The other problem is performance and energy overheads associated with entering and exiting sleep mode.

Unfortunately, traditional PG and BB have large sleep control overheads. Hence, those approaches can exacerbate energy dissipations if circuits enter into sleep mode during short idle periods.

According to previous work, the minimum sleep time to achieve leakage saving is ranges from tens to hundreds of processor cycles. On the other hand, many idle intervals appearing in sub blocks are spread ranges from tens to hundreds of processor cycles.
Thus, in order to reduce leakage power consumption in active processor, it is essential to reduce the sleep control overheads.

Multi-mode PG and BB are good candidates to perform leakage saving in Run-time. Each sleep mode has its own sleep depth. Deeper sleep mode provides higher leakage saving but incurs larger overhead energy.

For these techniques, increasing the number of sleep modes brings further leakage saving capability, however, it raises additional power consumption by bias generators which realize shallow modes. Therefore, we proposed static sleep depth control scheme which has only one shallow sleep mode and is able to reconfigure its depth in response to changing the running application or temperature. Our scheme is free from additional power of bias generators associated with the number of shallow modes.

Evaluation result shows that total energy saving for PG, traditional single-mode control, previous multi-mode control with 8 shallow modes and proposed control with 8 shallow modes achieve 24.5%, 34.0% and 33.5%, respectively. For BB with FBB case, achieve 7.7%, 24.3% and 23.4%, respectively. Our scheme using 8 shallow depths achieves almost same leakage saving efficiency as compared to ideal sleep control using 2 shallow sleep modes for both of PG and BB case. If overhead energy for bias generators is considered, our scheme takes advantage for power of additional bias generators.

Use of multiple modes is helpful for further leakage saving if an appropriate mode is selected, but the best mode depends on the idle period whose length cannot be told in advance.

Therefore, we proposed a novel sleep control scheme called stepwise sleep control scheme for multiple sleep mode techniques. Our scheme applies deeper sleep mode in a step-by-step manner according to elapsed time since idle state started. In run-time, it achieves efficient net leakage saving including overhead energy by applying appropriate sleep depth for various idle

intervals. Moreover, we proposed a methodology for optimizing depths and starting times of steps to maximize leakage saving. It adjusts depths and starting times according to run-time factors, temperature and idle interval distribution.

Evaluation result shows that proposed sleep control scheme improves net leakage saving of up to 23% with a geometric mean of 7% for FPAlu in the case of PG structure at 25deg. C. On the other hand, stepwise control achieves further saving of up to 63.7% with a geometric mean of 42.9% in the case of BB circuit. And result also shows increasing the number of stages from 2 to 3 improves 5¥% and 4¥% leakage saving for PG and BB case, respectively.