論文の内容の要旨

論文題目　Energy Efficient Design of Video Coding
Based on Harmonization of Hardware and Algorithm
（ハードウェアとアルゴリズム協調に基づく
エネルギー効率の高い映像符号化に関する研究と応用）

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The energy efficiency of digital circuits for mobile multimedia applications becomes increasingly important as larger numbers of transistors are integrated on a single chip. Multimedia technologies have enhanced the lives of mobile consumers by increasing productivity, enhancing the social networking experience, and delivering improved visual and audio quality for communication links and entertainment.

This work deals with an approach of how video codec processing can be integrated into energy efficient systems for smart society. In order to satisfy the high-performance and low-power requirements for advanced embedded systems with greater flexibility, it is necessary to develop parallel processing on chips by taking advantage of characteristics on video coding processing. This thesis explores high performance and low power technologies on video coding from both hardware architecture and video coding algorithm point of view.

The thesis is organized in the following manner. We start with a discussion on video codec design on semiconductor devices and systems. In particular, we

focus on low-power design to show the tradeoffs between high performance and low-power with respect to circuit performance, area, and flexibility to the multi format video.

Chapter 2 describes power-efficient video codec based on parallelism in the design. A two-domain (stream-rate and pixel-rate) processing approach raises the performance of both stream and image processing units for a given operating frequency. In the image-processing unit, a sophisticated dual macroblock-level pipeline processing with a shift-register-based ring bus is introduced. This circuit is simple yet provides high throughput and a reasonable latency for video coding. Stream processor and media processor architecture is also described for flexibility of video signal processing. It discusses the results of implementing circuits from the viewpoints of performance and power consumption.

Chapter 3 focuses on the problem of limited memory bandwidth. An over HD-video solution is still unable to target the today's handset market due to its high memory bandwidth and power consumption. Application specific techniques are proposed to improve the performance and power efficiency of DRAM by analyzing access patterns of video coding processing. With two parallel pipelines for macroblock processing and tile-based address translation circuits; the codec processor chip was implemented in 65nm CMOS. Power evaluation with dynamic frequency selection and changing operating voltage was conducted using 45nm CMOS technology. Proposal architecture even has extensibility for emerging video standards and outperforms homogeneous media processors in terms of performance

throughput and power efficiency.

As a result, the first Full-HD SoC available for handsets: 166 MHz mobile application processor is implemented in 65nm to support multistandard video codec at Full-HD resolution. 342 mW was achieved in real-time playback of a Full-HD H.264 High Profile stream from a 64 bit width low-power DDR-SDRAM at an operating frequency of 166 MHz at 1.2 V. This research created a positive economic impact for mobile applications that handset with Full-HD video recording and playback capability could be introduced to market in 2009 ~ 2010.

Chapter 4 looks into the important problem to interfere the parallelism in the video codec design. H.264/AVC is one of the most commonly used video compression formats for high definition video. It provide more flexibility for application than older standards such as MPEG-2 by adopting variable block-size motion compensation, spatial prediction from the edges of neighboring blocks for intra prediction, and context adaptive entropy coding. Foremost, inter and intra prediction scheme is developed separately. From the viewpoint of parallelism on hardware, it is the best solution that hardware can deal with all intra and inter picture prediction in a unified way. We propose a unification of intra and inter prediction based on template matching using repetitive pixel replenishment.

A new intra prediction method based on repetitive pixel replenishment (Intra RPR) is described. The concept of this proposal is unification of directional intra-prediction method and inter-prediction method. This intra-prediction scheme exploit motion vector search in a current picture, thus arithmetic logic unit for

template matching processing can share with inter prediction. Intra RPR method reduced the circuits' area by 19% of intra and inters prediction unit, and also Intra RPR outperforms H.264/AVC intra prediction by an average of 5.0% with a maximum of 10.3% BD-Rate improvement.

The methods proposed in this thesis applied in current 65 nm and 45 nm semiconductor technology, and demonstrate power efficiency in Full-HD video processing. The two-domain architecture is always applicable to the prospective semiconductor technologies. Unification of intra/inter prediction is the applied for emerging video coding standard that is based on DCT and motion compensation-based architecture toward a concrete goal to year of 2020 with Super-Hi Vision, i.e. 7,680 x 4,320 pixels, 60 frame/s, progressive scanning, 10/12 bit depth.