

## 論文の内容の要旨

論文題目 Control of Ultra-thin Amorphous High- $k$ /Ge Interface for Ge-CMOS Devices  
(Ge-CMOSデバイスのための極薄アモルファスHigh- $k$ /Ge界面の制御の研究)

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In the recent CMOS technology, device-size scaling and high-mobility channel are very important to achieve high-performance MOSFETs. To suppress short-channel effects in scaled MOSFETs, the equivalent  $\text{SiO}_2$  thickness ( $EOT$ ) of gate dielectrics should be scaled down to below 1 nm (subnanometer scale), in addition to suppression of interface states density ( $D_{it}$ ).

A high- $k$ /Ge gate stack is one of the most promising candidates for use in future CMOS devices. To achieve a high- $k$ /Ge with both subnanometer-scale  $EOT$  and low  $D_{it}$ , thermal stability and atomic diffusion at the interface are vital. Furthermore, amorphous high- $k$  gate dielectrics are also needed to suppress fatal gate-leakage currents. In this thesis, three types of amorphous high- $k$ /Ge interfaces are proposed, namely, (i) a reactive interface ( $\text{LaLuO}_3/\text{Ge}$ ), (ii) a less reactive interface ( $\text{Al}_2\text{O}_3/\text{Ge}$ ), and (iii) a nonreactive interface ( $\text{AlN}/\text{Ge}$ ). They are investigated at the desirable Ge-processing temperature of around  $600^\circ\text{C}$ , which is required to activate dopants in source and drain regions. Conventional thermal-equilibrium post-deposition treatments are also used to clarify the important factors that fundamentally determine the high- $k$ /Ge interface properties.

On the basis of these investigations, the guiding principles of  $EOT$  scaling and interface stabilization (low  $D_{it}$ ) in amorphous high- $k$ /Ge gate stacks are elucidated. First, an extreme suppression of  $\text{GeO}_2$  interface layer formation is proved to be of primary importance to achieve

subnanometer-scale  $EOT$ . Second, the stabilization of a  $\text{GeO}_2/\text{Ge}$  stack (suppression of  $\text{GeO}$  desorption) with the use of rare-earth metal, Al, and N atoms is determined to be pivotal to achieve a low  $D_{it}$ . In the process, some new findings on high- $k/\text{Ge}$  gate stack processing are also discussed. Finally, a high- $k/\text{Ge}$  gate stack with an  $EOT$  of  $\sim 0.88$  nm and a  $D_{it}$  of  $\sim 10^{11}$   $\text{eV}^{-1}\text{cm}^{-2}$  is successfully demonstrated.

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