論文の内容の要旨

論文題目: Study of Ge Interface Control for Realizing High-Mobility Ge CMOS

(高移動度 Ge CMOS の実現に向けた Ge 界面制御の研究)

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As aggressive scaling of conventional Si device approaches its fundamental limits, novel materials with better electrical properties are being intensively researched. Ge has a big advantage over Si in terms of high electron and hole mobilities, and its low processing temperature makes it easier to integrate with high-*k* materials. However, Ge has suffered from the absence of a stable oxide on Ge unlike Si/SiO_2 because it is well known that the Ge/dielectric interface easily deteriorates due to GeO desorption during thermal processing. Despite the enormous progress in Ge surface passivation, the electrical properties of Ge/dielectric interface does not meet the requirements of electronic device. In order to realize high-performance Ge CMOS, devices and process issues have to be thoroughly investigated. In this thesis, we have focused on how to improve Ge/GeO_2 interface properties and electron mobility in Ge n-MOSFETs, which are an urgent need for realizing high-mobility Ge CMOS.

To reduce the Coulomb scattering sources in Ge gate stack, the formation of high-quality Ge/GeO_2 gate stack by high-pressure oxidation (HPO) was investigated. The capacitance-voltage characteristics of metal/GeO_2/Ge capacitors fabricated with HPO revealed the improved electrical properties. It is also discussed from a thermodynamic viewpoint of the Ge/GeO_2 stack that the GeO desorption from Ge/GeO_2 stack could be efficiently suppressed by

HPO. Low-temperature oxygen annealing (LOA) was proposed to further reduce the interface states density (D_{it}) and a new concept to Ge thermal oxidation was suggested by using the two-step oxidation (HPO and LOA). Furthermore, the impact of rare-earth inclusion in Ge/GeO_2 stack was discussed in terms of interface passivation. On the basis of our understanding about Ge/GeO_2 interface, the highest electron and hole mobilities in Ge MOSFETs were demonstrated with Ge/GeO_2 gate stack. This can be achieved by taking care of thermodynamic and kinetic control of Ge/GeO_2 interface.

The mobility universality in Ge MOSFETs was examined for understanding the mechanisms of mobility degradation, and the effects of surface roughness on electron mobility in Ge/GeO_2 n-MOSFETs were experimentally investigated to determine the dominant scattering source for the high-E_{eff} electron mobility. It was found that the significant degradation of electron mobility in the high-E_{eff} region is not simply determined by the surface roughness scattering, and an additional scattering mechanism, which is not necessary to consider in Si MOSFETs, might be involved in the electron transport in Ge n-MOSFETs. The major scaling issues for realizing high-mobility Ge CMOS were discussed and possible solutions were presented. For the equivalent oxide thickness (EOT) scaling of gate stack, we examined the low-temperature high-pressure oxidation for scaling the Ge/high-*k* dielectric and sub-nm EOT of $Ge/GeO_2/Y_2O_3$ stack with very low D_{it} and gate leakage current was achieved. We also investigated the ultrathin GeOI n-MOSFETs in terms of carrier transport, and revealed that electron mobility in ultrathin body GeOI MOSFETs is limited by GeOI crystallinity near BOX (Ge/SiO_2). The origin of reverse leakage current in n^+/p junction was characterized by Raman scattering measurement. It is found that Ge bulk crystallinity is not fully recovered from the implantation damage despite the dopant activation at high temperature.